THESIS SUMMARY

Current trends in electronic design have led to the miniaturisation of systems. This is especially true in the field of portable equipment design. However, in many cases the component which occupies the most volume is the power source for this equipment.

The large volume of the power source is due to the size of the magnetic components which they contain. It is essential to reduce in size or replace these components with adequate alternatives to decrease in size the power source.

There exists an ongoing pursuit for new technology for the replacement and miniaturisation of magnetic transformers with components that have the same characteristics (electric isolation, voltage step), or in other words transformers which allow a higher power density.

Piezoelectric Transformers (PT), based on mechanical coupling, are becoming a promising alternative for magnetic transformers. This is due to their many inherent advantages, such as:

- **High power density.** With adequate transformer designs, it is possible to achieve higher power density levels, which are greater than those obtained from magnetic transformers.
- **High voltage gain** which permit high voltage conversion with higher power densities than those obtained magnetic transformers.
- **Low levels of electromagnetic interferences (EMI)**, as mechanical vibration energy is an important part in the transference of energy and not the magnetic flow.
- **High levels of electric isolation** this is an important factor when considering applications where there exists a high difference between the input and output voltage levels.

Even though the first mechanically coupled transformers were proposed in the 1950's (*Rosen* type transformers), until now no commercial applications have been developed. This is due to deficiencies in the characteristics of the materials (aging, high losses, etc.).

Due to the development of new structures, new functioning methods, and the introduction of piezoelectric materials with improved characteristics, PT may now be used in many diverse commercial applications, including the field of power sources with high output voltages. In particular, Rosen type transformers are used as power sources for liquid crystal displays (LCD) in portable electronic equipment (video

cameras, computer monitors etc..). Such applications require high output alternating voltages (1200 V_{ef}) in comparison to the continuous voltage at the input (5 to 9 V). Since the output of such devices is alternate, and rectification of the signal is not required, the specifications of the converter are comparable to applications which use magnetic components (80%, for power levels between 0.5 and 1.5 W). These converters are shown to have smaller dimensions (2.3 mm) than those composed of magnetic components (3.5 mm). Using PT gives the required low EMI levels which comply with the regulations applied to these types of electronic systems.

This thesis focuses on low output voltage DC-DC converters, as currently no commercial products contain such PTs. The main reason for this lack of commercialisation is that the results obtained from such devices are not competitive in comparison to those developed using magnetic components. Of the many applications in this field it is worth mentioning commonly used products such as battery chargers for portable computers and mobile phones as well as *on board converters.* Telephones and laptop computers are shown to be constantly reducing in size whereas the chargers for their batteries do not. *On board converters* are power supplies which are found within the telecommunications card, as a result their size should be reduced.

Currently two different methods exist in the development of PT based DC-DC converters.

The traditional method is centred on the optimization of the transformer output and size of the PT. In this case, the PT is governed by a sinusoidal voltage at a frequency which is equal to the resonance frequency of the components. However, in order to generate these types of voltage waveforms, it is necessary to include in the topology of the converter, additional magnetic components in both the input and output stages of the PT. As a consequence, the advantages are significantly reduced with respect to finding new technology for replacement of magnetic transformers.

The other alternative, which is proposed in this thesis, consists of designing a PT for square wave voltages with soft switching. In this way, all magnetic components can be removed from the topology. As a result, optimization of the converter is sought, although this implies that the behaviour of the PT is less efficient than the aforementioned method.

> *In this Thesis a new methodology for the design of Piezoelectric Transformers (PT) which will allow the optimization of the complete conversion process. This methodology has been applied to switch mode AC-DC or DC-DC power supplies with low power and low output voltage. In order to achieve this, adaptation of existing electronic models is required; in such a way that they result adequate for the design of the PT. Using such models a design procedure and new geometric structures of the PT have been established. This analysis has improved*

the performance of the DC-DC converter, showing the possibility of reducing, even eliminating, the magnetic components.

As well as working on the design of the PT, a proposal for improvements from the point of view of the converting topology is presented. In order to evaluate the advantages of the methodology of the proposed design, the obtained results have been compared to existing commercial solutions with magnetic components. All these aspects have been experimentally validated with the construction of various laboratory prototypes.

In the **first chapter** a description of the working principles of the PT is presented. This includes parameter definitions which are fundamental for the design of the component. A global vision of the state of the art with regards to current usage of PT is also given. For the applications under investigation, i.e. low output voltage, PT with various secondary layers are required (multilayer structures). Of the various different existing PTs currently available. This Thesis centres on PTs which employ a vibration throughout the thickness of the component for transferring the energy (thickness mode).

In the **second chapter** an evaluation of the requirements to which the PT model must comply with is outlined, this is required for efficient design and integration of the component in the power converter.

The analytical solution of the equations which define the behaviour of the PT is a very involved process as it is a three dimensional system (3D). In order to reduce the complexity of this model simplifications are made. Currently there exist models which only take into account the principal vibration direction. These models are known as one-dimensional models (1D). Such 1D models permit an analysis of the behaviour of the PT with the rest of the components in the topology, as their implementation in commercial electric simulators is a straightforward process. The majority of the designers employ this type of model to define the constructive parameters corresponding to the principle direction in which the vibration of the PT is produced.

However the behaviour of the PT is very dependant on its 3D shape. This is due to the influence of unwanted vibrations in other directions apart from those involved in the energy transfer process. As a result, the scope of the 1D model is limited when no account of the influence of the external geometry of the PT is taken. Finite element analysis (FEA) tools permit simulation of these effects; however they do not generate an electrical model. This Thesis presents **an original method for establishing the parameters of the 1D model**, which is valid for the type of structures considered in this research work. These parameters are obtained **from the information given by FEA tools or by the measurements carried out in the PT** ([1],[2]).

This is followed by the **third chapter**, where the improved model described in chapter 2 is used to employ an **original procedure for the design of the PT from the electric specifications of the power converter topology** ([3],[4]). This design process is based on the application of the rules obtained from an analysis of the sensitivity of the constructive parameters from the 1D model [5]. These rules permit an efficient selection of the new dimensions of the PT for any changes in the electrical specifications, thus reducing the design time. Also, it is necessary to make use of the FEA tools for an adequate selection of the PT external geometrical shape.

An original proposal for the internal distribution of the electrodes of the PT is described. This is based on **the interleaving of the primary and secondary electrodes of the component** ([6],[7]). The new distribution of the electrodes has produced many advantages when compared with the electrode configurations used to date. It is important to highlight the possibility to remove the magnetic components from the DC-DC converter topology.

Finally, **a study and proposal of a new method for mounting the PT on the converter board has been performed** [3], given that it is a basic aspect in the performance of this component. Its behaviour is dependant on the mechanical conditions, since the energy transfer is produced via mechanical vibrations. If the mounting method is not adequate, limitations on the movement and resistance to the transferral of energy in the PT are present. The proposed support method, compared with the evaluated systems, also gives an optimization of the access to the electrical connection terminals of the PT.

Apart from the design of the PT, a study of different aspects related to the scheme of the power stage has been carried out.

In the **fourth chapter** the different **alternatives to drive the PT have been compared**, this gives knowledge of the advantages and disadvantages for each one of these. Thus **allowing selection of the most adequate option for each possible application** [8].

The selection of the working frequency of the switches in the inverter stage of the DC-DC converter is determined by the PT. In order to obtain high power density in the component, the working frequency should be high. However, this frequency penalizes the switching losses of the power stage.

In this Thesis, **an original proposal** for driving the PT at frequencies lower than the fundamental (**subharmonic driving** [9]) is presented. This form of driving gives rise to the possibility of reducing the working frequency of the switches in the inverter stage while the working frequency of the PT remains high. This gives a reduction of switching losses in the power topology.

In the **fifth chapter,** a comparison of applications using PT, within the field of study, with commercial applications originally developed using magnetic components is performed. Two commercial applications with low output voltages have been selected. These are the aforementioned: battery charger for mobile telephones and *on board converter*. From this analysis, the possibility of a competitive converter based on PT is demonstrated. This is due to adequate component design which allows the elimination of all magnetic components in the DC-DC converter topology.

Taking into account the conclusions of the previous chapter, the **sixth chapter describes the construction of a DC-DC converter without any magnetic components** [10]. The results obtained show the viability of the PT in the applications under investigation, enforcing that there is no need to introduce any additional magnetic components. For a constant input voltage, the power and the performance of the developed application are 3.2W and 73% respectively. These results are greater than those obtained for the case of an application with a wide input voltage range (1:3.75), which has a performance of 60% at a power of 1W.

Finally, in the **seventh chapter,** the advances described throughout this doctoral Thesis are presented. Apart from the results obtained, indications to further and future work in this research area are presented.

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1D Modeling of Multi-layer piezoelectric transformers

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Abstract-This paper presents a general procedure to obtain 1D models of multi-layer piezoelectric transformers. A detailed description of how to model the different parts of the transformer: active layer, bulk material, connection and mechanical restrictions is given. Temperature effect on piezoceramic properties is taken into account. Simulated and measured results are also presented.

I. INTRODUCTION

Piezoelectric transformers (PT) are becoming a good alternative to magnetic transformers in some particular applications, especially in those cases in which high voltages and high isolation levels are required. Electrical energy in PTs is transferred through mechanical vibration and power densities higher than that of magnetic transformers are obtained. Not only smaller size and weight are achieved, but also lower EMI emissions due to its energy transfer mechanism. These characteristics are making these devices very attractive for low power DC/DC and AC/DC converters

Design of multi-layer PTs is not an easy task, even if a 1D approach is followed. Several factors as the poling direction, layer interconnection, temperature and electrodes connection can influence the behavior of the PT. Consequently, in order to predict the behavior of the PT, it is necessary to be able to model all these kind of elements simultaneously.

This paper presents a procedure to obtain 1D models of multi-layer PTs in circuit oriented simulation programs such as SPICE. A detailed description of how to model active layers, bulk material, connections and mechanical restrictions is also provided. Temperature effect on piezoceramic parameters is also accounted for.

This modeling approach is not only useful due to important electrical design parameters such as input impedance, output impedance and transfer functions can be easily obtained by means of a frequency analysis performed by the simulator, but also mechanical design restrictions, such as maximum stress and strain, can also be easily checked.

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II. MULTI-LAYER PIEZOELECTRIC TRANSFORMER MODELING

A. Piezoelectric Layer

Several works have been published related to 1D modeling of piezoelectric layers [1,2]. These models are based on a one-dimensional wave propagation along one of the axis, as it is illustrated in Figure 1a. It is also assumed that the electric field intensity, E, and the electric displacement, D, are also in the same direction.

According to this, and taking F as the mechanical force, U the particle velocity, I the current through the layer and V the voltage across the terminals, the wave equations can be expressed as follows [1-3]:

$$\frac{\partial}{\partial z}\left(F(z,s)-\frac{h}{s}I(s)\right)=-\rho AsU(z,s) \qquad (1)$$

$$\frac{\partial}{\partial z}U(z,s)=-\frac{s}{Ac}\left(F(z,s)-\frac{h}{s}I(s)\right) \qquad (2)$$

and the voltage can be expressed as:

$$V(s)=\frac{h}{s}\left(U_1(s)-U_2(s)\right)+\frac{1}{C_o s}I(s) \qquad (3)$$

where A is the cross-sectional area perpendicular to the wave direction, h is the piezoelectric constant, c is the relative elastic constant, ρ is the density and s is the Laplace variable.

Figure 1b shows an equivalent electrical circuit model that can be used to represent equations (1),(2) and (3). Mechanical force and particle velocity are represented by voltage and current respectively. A symbol for this active layer is shown in Figure 1c.

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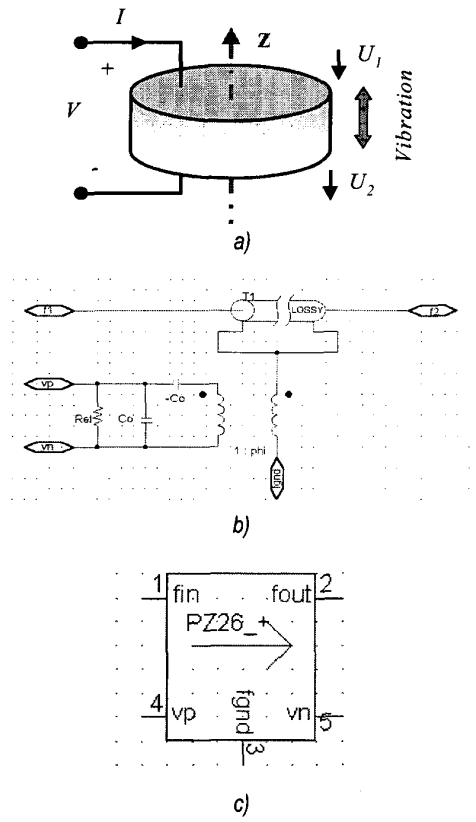


Figure 1. a)Thickness mode piezoelectric layer b) Equivalent circuit. c) symbol

The circuit consists of:

- Static capacitance(C_o) that represents the capacitance between the electrodes.
- Transmission line, T1, that represents the mechanical part of the piezoelectric material.
- Ideal transformer and negative capacitor ($-C_o$), that represent the coupling between the electrical and mechanical part.
- Nodes *fin*, *fout* and *fgnd* represent mechanical connections of the layer to the previous, next and reference force nodes respectively.
- Nodes *vp* and *vn* stand for the electrical connections of the active layer, the electrodes.

The equivalent electrical circuit model parameters are given by:

$$C_o = \varepsilon_{33}\frac{A}{d} \quad (4)$$

$$phi = \varepsilon_{33}\frac{A\cdot h}{d} = C_o h \quad (5)$$

$$L = \rho A \quad (6)$$

$$C = \frac{1}{A\cdot c} \quad (7)$$

where L and C are the transmission line inductance and capacitance per unit length respectively and ε_{33} the dielectric constant in the movement direction.

Losses in piezoelectric materials are of two different origins, mechanical and dielectric. Mechanical losses can be modeled in the transmission line. Dielectric losses can be modeled in the electrical part of the circuit.

Mechanical losses can be accounted for as in [4]. It is assumed that the quality factor, Q, for solid materials without scattering is constant with frequency. Where the quality factor is defined as:

$$Q = \frac{\omega L}{R} \quad (8)$$

A constant quality factor implies the use of frequency dependent resistance in the transmission line, that in the case of AC analysis works fine but running a transient analysis can cause convergence and non-causality problems.

Dielectric losses can be taken into account by making use of a complex dielectric constant ε_{33}. This can be translated into the use of a resistor in parallel with Co.

$$\varepsilon'_{33} = \varepsilon_{33}(1 - j\cdot tan\delta_e) \quad (9)$$

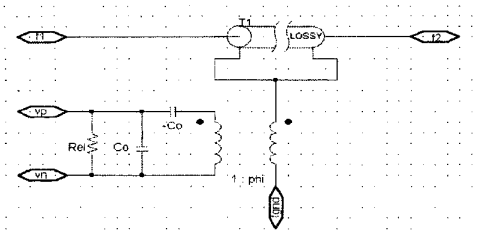
$$R_{el} = \frac{1}{\omega C_o tan\delta_e} \quad (10)$$

The problem of this approach is that if a constant resistance is used, the electric loss factor, tan δ_e, will be frequency dependent. In order to solve this problem, a frequency dependent resistor should be used. This can be easily done by means of a frequency dependent voltage controlled current source. Nevertheless, this frequency dependence can cause problems in transient simulations. If the piezoelectric is intended to work in a narrow frequency range, a constant resistance can be employed calculated for the center frequency of this range.

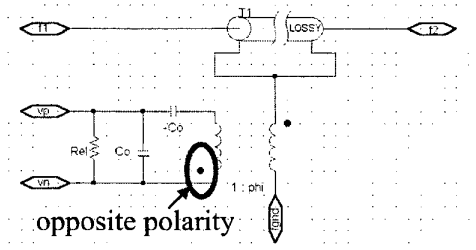
B. Poling

Poling direction is especially important in multi-layer piezoelectric transformers since it can radically change the behavior of the component. Paralleled layers should be connected in such a way that the electric field is applied in the same poling direction.

Poling direction can be taken into account by changing the polarity in the transformer that couples the electrical and mechanical portion of the piezoelectric layer as shown in Figure 2. If the coupling between the mechanical and electrical part were modeled by means of dependent sources [3] and [4] it would be necessary to change the sign of one of these dependent sources.



a) forward poling



b) inverse poling

Figure 2. Poling modeling. a) Forward poling. b) Inverse poling.

C. Bulk material

Frequently, multi-layer piezoelectric transformers consist on a primary and a secondary made of stacked active layers and a passive material, known as bulk material, that is introduced in order to fix the resonance frequency. It is usually the same piezoceramic material as the active layers but it is not poled. As there is not electrical-mechanical interaction, it can be modeled as a lossy transmission line, shown in Figure 3, representing the mechanical part (1) and (2).

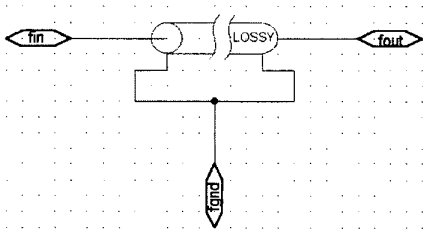


Figure 3. Bulk material equivalent circuit model

D. Mechanical fixing

The PT needs to be fixed to the PCB. Both the fixing and its location can considerably affect the behavior of the PT, changing the resonance frequency, the coupling factor, the gain and all its parameters. Any other 2D effect that could show up, would not be predicted by this model such as the appearance or moving of resonances different than the produced along the main vibration axis.

Since an equivalence between mechanical force and electrical voltage, and, mechanical velocity and electrical current, has been established, it is possible to represent mechanical relationships between force and velocity as electrical relationships between voltage and current. Basic mechanical elements can be represented by their electrical counterparts.

Mechanical	Electrical
Spring: $F = K\int u \cdot dt$	Capacitor: $V = \frac{1}{C}\int I \cdot dt$
Damping: $F = B \cdot u$	Resistor: $V = R \cdot I$
Mass: $F = m\frac{du}{dt}$	Inductor: $V = L\frac{dI}{dt}$
Free end: $F = 0$	Short-circuit: $V = 0$
Fixed end: $u = 0$	Open-circuit: $I = 0$

Table 1 Equivalent mechanical-electrical

Taking into account the equivalence between mechanical and electrical quantities, shown in Table 1, the mechanical fixing can be easily modeled by means of a passive network. In this network, the inductor models the mass, the capacitor stands for the inverse of the elastic constant, and finally the resistor models the viscosity and internal losses.

In the case that one of the ends were free to move, this could be modeled by means of a zero voltage source indicating that there is not mechanical force reaction in this end. The opposite case would be one of the ends totally fixed. This can be modeled by means of a zero current source (open-circuit), meaning that the particle velocity in this end is zero.

III. TEMPERATURE EFFECT

Temperature plays an important role in the behavior of the PT. Especially important is the dependence on the temperature of the relative dielectric coefficient at constant stress, k_{33}^T ($\varepsilon_{33}^T = k_{33}^T \varepsilon_0$), and the dielectric losses tangent, $\tan\delta_e$. Actual data for different kinds of PZT ceramics showing the dependencies of those properties with temperature have been extracted from [7] and they are presented in Figure 4. It can be noticed how both parameters, k_{33}^T and $\tan\delta_e$ increase with temperature.

In order to account for this effect the temperature is defined as a global parameter. Dielectric constant, ε_{33}^T, and losses tangent, $\tan\delta_e$, are defined as functions of the temperature. An exponential curve fitting of the form, $y = a\,e^{bT}$, has been used to approximate the dependence of the dielectric constant and the losses tangent on the internal temperature of the component. This allows performing parametric analysis of the temperature in order to evaluate how this affects the efficiency of the PT. An example of the influence of the temperature on the efficiency is shown in Figure 5.

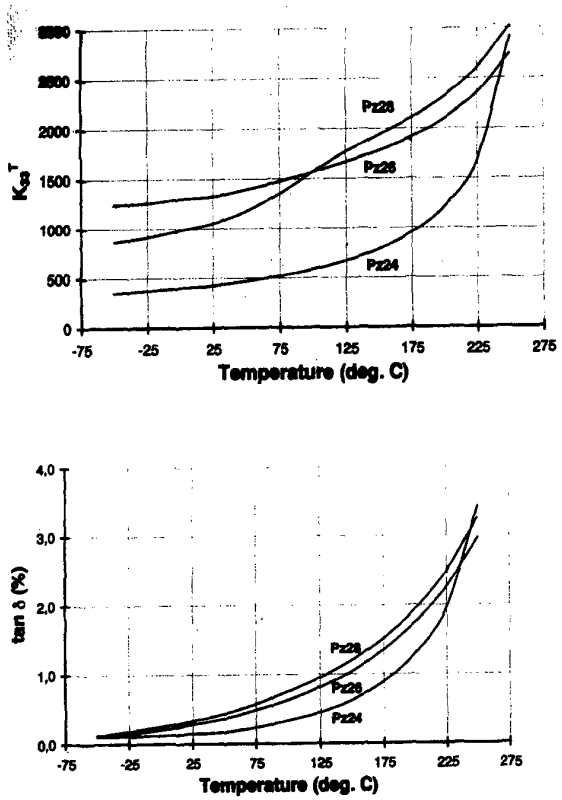


Figure 4. ε_{33}^T and tanδ vs temperature in Celsius degrees

It is interesting to note how the dependence of these parameters with frequency have opposite effects on the efficiency of the piezoelectric transformer.

On one hand, if the dielectric constant is increased, as it happens when the temperature raises, keeping the dielectric looses tangent constant the efficiency of the PT would increase. This, surprisingly, would mean that efficiency would increase with temperature.

On the other hand, if the dielectric constant is fixed and the dielectric losses tangent is increased the efficiency would decrease. This result is closer to what it is expected. When both values are changed, according to their actual values, it can be seen (Figure 5) that as the temperature increases the efficiency decreases around the resonance frequency.

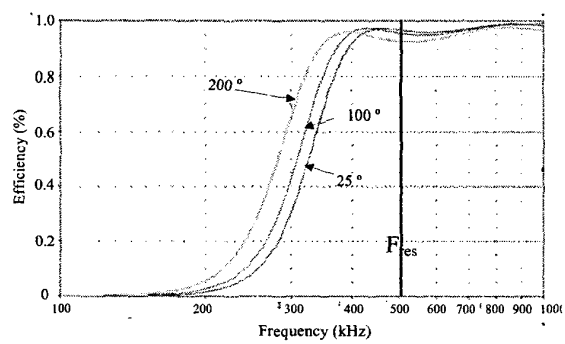


Figure 5. Efficiency vs frequency at 25, 100 and 200 °C

IV. APPLICABILITY OF THE MODEL

This modeling approach has been successfully applied in the design of piezoelectric transformers for DC/DC power converters. It helps the designer to focus on electrical parameters such as input impedance, output impedance, voltage gain and efficiency.

A general procedure to design PTs is given in [6]. Several parameters have to be adjusted in order to obtain a proper design and they can be summarized as follows:

- The optimum load of the PT, load at which it has maximum efficiency, should be close to the application load.
- Input conductance should be higher than the needed to transfer the maximum power.
- Efficiency and electromechanical coupling as high as possible.
- Physical limitations: stress, strain, electric field and electric displacement should be bellow the maximum allowed.
- Temperature rise should be kept bellow some certain value.

Figure 6 shows the behavior of two different PTs vs frequency. From a frequency analysis like this, the designer can extract valuable information related to the design:

- The higher the coupling coefficient, K_{eff}, the higher the working frequency range (between resonance and anti-resonance frequencies).
- Input impedance phase is higher for the design of higher K_{eff}. This means that the ZVS implementation is more feasible.
- For higher K_{eff} the variation of the input conductance is higher, so that, this design admits more variation in the input voltage.

Since the variation of constructive parameters and material properties have a great influence on the behavior of the piezoelectric transformer, sensitivity analysis can be carried out in order to check which are the critical points of the design.The same model can be used to analyze those points.

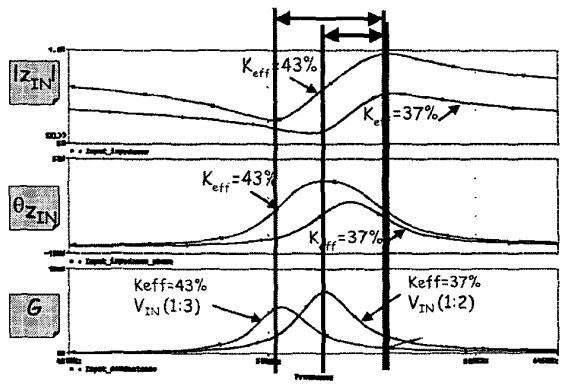
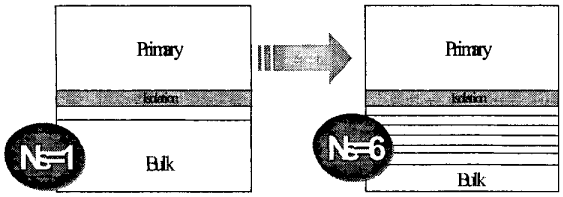
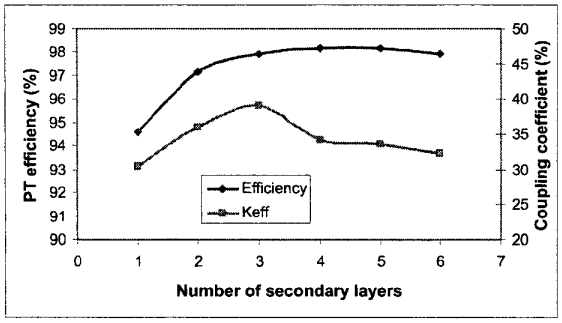


Figure 6. Module,$|Z_{IN}|$, and phase, θ_{IN}, of the input impedance and input conductance, G, vs frequency for two PTs with different effective coupling coefficients.



a)



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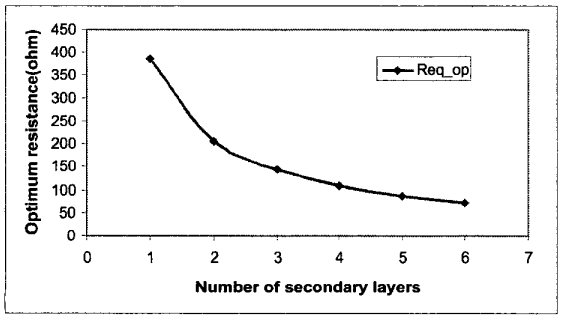


c)

Figure 7. Effect of the number of secondary layers.
a)Structure with for 1 and 6 layers.
b) Efficiency and coupling coeff. vs number of secondary layers.
c) Optimum resistance vs number of secondary layers

Figure 7 shows how the number of secondary layers affects important parameters such as the efficiency, the coupling coefficient and the optimum load resistance. Similar analysis can be easily performed changing the area, the primary, the strategy.

V. MODEL VALIDATION

This modeling approach has been validated and it also has been employed in the design of several PTs for power converters.

In order to illustrate the accuracy and the usefulness of the modeling approach, one of these cases is presented. Figure 8 shows the structure of a patented 10W PT [8].

The PT consists on a one-layer primary and an eight-layers secondary, two floating layers, an insulation layer and two bulk zones to adjust the resonance frequency. Secondary layers are connected in parallel, and the primary is located inside the two floating layers that are short-circuited. This structure is used in order to reduce the thickness of the isolation layer. The purpose of reducing the thickness of the isolation layer was derived from the sensitivity analysis carried out on this parameter. It was shown that the efficiency of the piezoelectric transformer decreases as the isolation layer thickness increases.

The equivalent circuit for this structure is illustrated in Figure 9, where it can be observed the location of the bulk at both ends, the mechanical connection of the layers, their poling directions, and the electrical connections between electrodes.

This equivalent circuit is not only useful for determining the main parameters of the piezoelectric transformer under any kind of load or mechanical condition. But, it also can be inserted into the whole power electronic converter in order to evaluate the global behavior of the system.

The input impedance of such PT loaded with a 17Ω resistor has been measured and simulated (Figure 10). A good agreement between the actual and theoretical behavior has been obtained. The measurement shows more resonance frequencies that are due to additional modes of vibration, other than the thickness mode, that are not taken into account by the 1D model. This can only be observed by means of FEA simulation. PT's are usually designed to keep these additional modes far enough from the main resonance frequency in order to obtain a better energy transfer, so 1D models will describe very well the behavior of these devices.

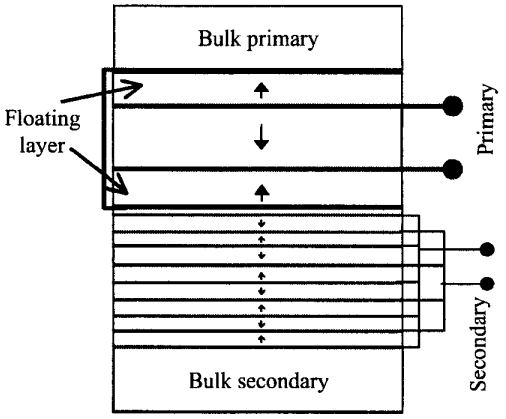


Figure 8. Modeled PT structure

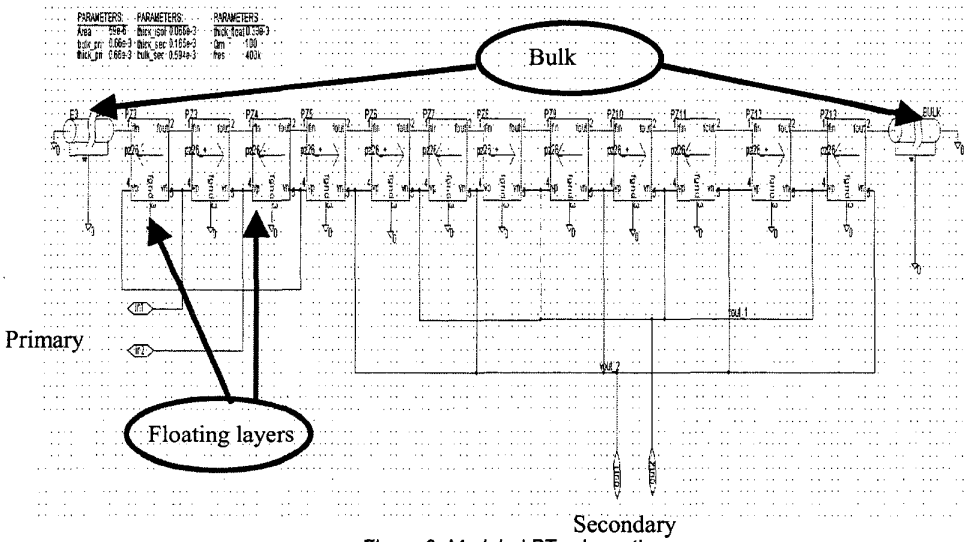
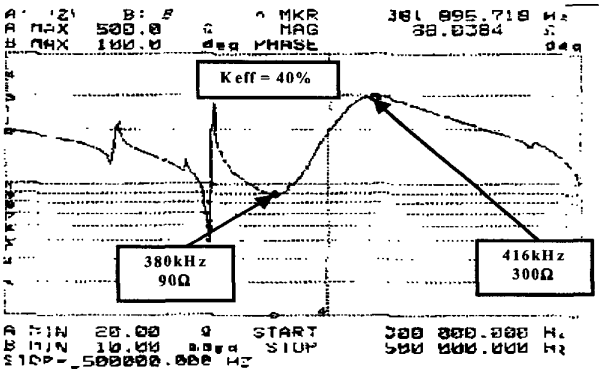
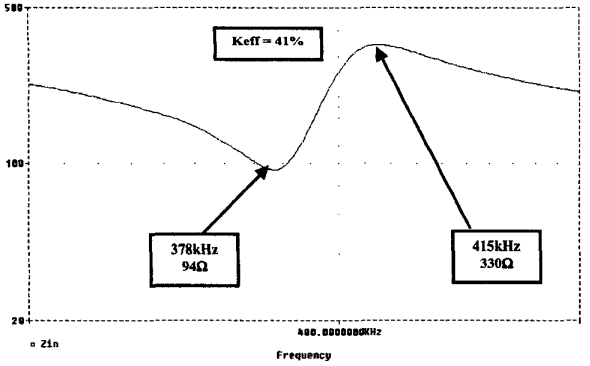


Figure 9. Modeled PT schematic



a) Measured



b) Simulated

Figure 10. Measured vs simulated input impedance

VI. CONCLUSIONS

A general procedure to obtain 1D models of multi-layer piezoelectric transformers has been developed. A detailed description of how to model the different parts of the transformer: active layers, bulk material, connections and mechanical restrictions is also provided. Temperature effect on material properties has also been accounted for.

These models are suitable to be implemented in circuit oriented simulation progams such as SPICE. This provides high flexibility since the same models used in the PT design can be used in the analysis and design of the whole electronic system in which the PT is included.

Experimental and simulated results have been presented showing the validity of the derived model.

ACKNOWLEDGMENTS

The authors would like to thank Rafael Asensi for his help in the programming of an automatic tool for the design of piezoelectric transformers.

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FEA based Model of Multi-layer Piezoelectric Transformer working in Thickness Mode

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Abstract— Piezoelectric Transformer (PT) design requires Finite Element Analysis (FEA) tools, because its performance depends strongly on its shape (2D/3D effect). The main drawback of these tools is that they do not provide the electrical model needed to design the power converter. Nevertheless, the existing electrical models only take into account the main direction of vibration (1D). In this paper, a procedure to improve 1D model parameters by taking into account FEA tool information is proposed.

I. INTRODUCTION

Nowadays, Piezoelectric Transformers (PTs) are attractive compared to magnetic transformers to reduce size and weight in AC/DC and DC/DC converters for low power and low output voltage where these features are critical issues [1]. Not only smaller size and weight are achieved, but also lower radiated noise due to electrical energy is transferred through mechanical vibration. In addition, higher isolation voltage levels are obtained.

Thickness vibration mode has been selected to obtain a low profile converter. It is important to highlight that the low load (several ohms) of the considered applications requires the use of multi-layer PT structures to obtain high PT efficiency.

Electrical PT models can be used in circuit oriented simulation programs such as SPICE. This modeling approach is useful not only for determining the main parameters of the PT. But, it also can be inserted into the whole power converter in order to evaluate the global behavior of the system and to realize proper converter design [2].

A suitable electrical model for multi-layer PT working in thickness mode has been described in [3]. However, this model is one-dimensional (1D) since it only takes into account the main vibration mode. But, the performance of the PT is strongly dependent of its shape (3D). Since mathematical equations are very difficult to resolve analytically in a 3D system, Finite Element Analysis (FEA) tools are needed. Although this analysis allows taking into account complete PT performance, it is not enough since no electrical model is obtained.

Hence, in this paper, a procedure to extract 1D model parameters for multi-layer PT working in thickness mode including FEA tool information is proposed.

[1] Currently she is assistant professor at Universidad Carlos III de Madrid

II. MODELING REQUIREMENTS

Models of Piezoelectric Transformers (PTs) are required in order to design DC/DC converter based on PTs (figure 1).

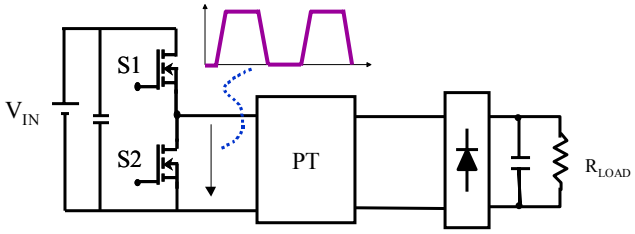


Figure 1. DC/DC power converter topology based on a PT.

Electrical PT requirements should be determined by considering topology restrictions in order to optimize the power converter. Therefore the PT model should take into account several requirements that are described below.

- **Easy to implement in an electrical simulator**

An electrical PT model is required in order to include it in the whole power electronic converter and to realize proper converter design.

- **Analysis of the main vibration mode**

The PT transfers the electrical energy by the vibration along one main selected direction. Therefore, the model must take into account the electrical behavior of the PT in this direction. In this paper, the thickness is considered as the main vibration direction.

- **Analysis of the higher orders of main vibration mode**

Square driving with soft transitions (figure 1) allows optimizing the power converter by avoiding additional magnetic components required for impedance matching at the input of the PT, as analyzed in [4]. That means that the driving voltage contains higher order harmonics of the PT resonance frequency. If the harmonic content of input PT voltage drives the higher order harmonics of the PT, lower PT efficiency is obtained.

- **Analysis of spurious modes**

Proper PT design must be cleaned of other vibration modes, named as spurious modes. The spurious modes make the PT vibrate in different and non-desired directions, which implies a reduction in the PT efficiency.

- **Analysis of the losses**

PT efficiency must be high enough to obtain the specified value of converter efficiency.

In addition, PT losses require a minimum component volume to limit its temperature rise since this magnitude should be kept below some certain value that makes the piezoelectric material changes its behavior.

- **Analysis of fixing**

The PT needs to be fixed to the PCB. Both the fixing and its location can considerably affect the performance of the PT, since the electrical energy is transferred by mechanical vibration.

- **Analysis of the electrode distribution**

Multi-layer PT structures are more appropriate to obtain high PT efficiency for the low load values required (several ohms) by the considered applications.

As analyzed in [5], this feature is very important from the point of view of PT converter since proper electrode distribution allows designing PT to provide ZVS condition without additional magnetic components.

- **Electromechanical coupling (k_{eff}) as a function of PT shape**

This parameter is very important not only for component design, but also for power converter design.

As shown in equation (1), k_{eff} has strong influence on PT power density (Power/Volume).ε is the material permittivity and f is the vibration frequency [6].

$$\text{Power}/\text{Volume} \propto k_{eff}^2 \cdot \varepsilon \cdot f \quad (1)$$

This parameter determines the operating frequency range of the power converter by equation (2) where f_{res} is the resonance frequency and f_{ares} is the antiresonance frequency of the PT [7].

$$k_{eff} = \sqrt{\frac{f_{ares}^2 - f_{res}^2}{f_{ares}^2}} \quad (2)$$

The switching frequency of the converter is placed between f_{res} and f_{ares}, where PT transfers the energy efficiently and is able to provide ZVS without additional magnetic components [4].

III. MODELING ALTERNATIVES

This section evaluates the different modeling alternatives of PTs in terms of the requirements described in section II.

Existing electrical PT models are based on a one-dimensional (1D) wave propagation along one of the PT axis that is the direction of the main vibration mode.

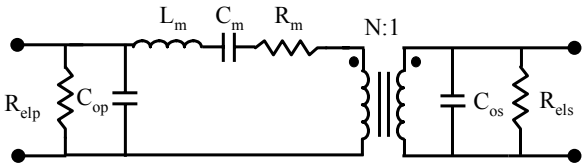
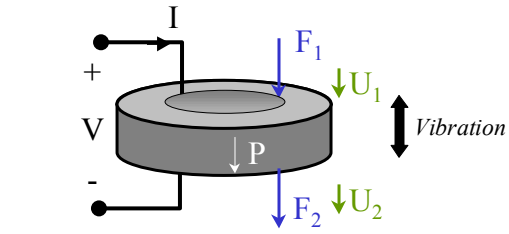


Figure 2. Mason model of a Piezoelectric Transformer.

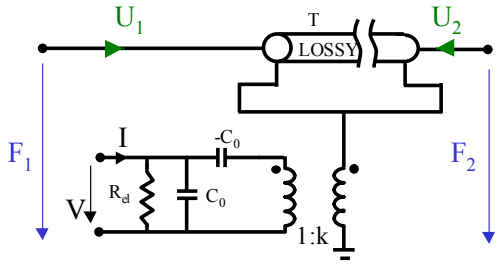
Usually, PT designers ([8], [9]) use Mason model [10] due to its simplicity. The structure of this model is shown in figure 2. Mechanical losses are modeled by the resistor R_m and dielectric losses are modeled by a resistor (R_{elp} and R_{els}) in parallel with the capacitance of primary (C_{op}) and secondary (C_{os}) PT side respectively.

Nevertheless, Mason model is only valid when PT is sinusoidally driven because it only takes into account the main vibration mode of PT. In addition, fixing conditions and electrode distribution are not taken into account.

The electrical PT model based on transmission lines ([11], [12]) takes into account the higher orders of the main vibration mode. Furthermore, this model is more appropriate to predict the behavior of a multi-layer PT because it is able to considered different fixing conditions, poling and position of the layers since each layer is modeled independently. Figure 3.b shows the model parameters for a single layer of piezoelectric material (figure 3.a). F_1 and F_2 as the mechanical forces at each side of PT layer, U_1 and U_2 are the particle velocity at each side of PT layer, I is the current through the layer and V the voltage across the terminals. Equivalent electrical circuit is obtained by representing mechanical force and particle velocity by voltage and current respectively.



a. Layer of piezoelectric material



b. Model parameters

Figure 3. Transmission line model (b) of a layer of piezoelectric material (a) working in thickness mode

The equivalent circuit consists of:

- Static capacitance (C_o) that represents the capacitance between the electrodes.
- Transmission line, T that represents the mechanical part of the piezoelectric material. Mechanical losses can be modeled in the transmission line.
- Ideal transformer, with a transfer ratio named as k, and negative capacitor ($-C_o$) that represent the coupling between the electrical and mechanical part.
- A resistor (R_{el}) in parallel with Co that takes into account the dielectric losses.

The expressions of these parameters are detailed in section IV.

However, model based on transmission lines is a 1D

model. Therefore, spurious modes and suitable value of k_{eff} are not obtained.

Finite Element Analysis (FEA) tools are required to take into account PT shape (figure 4). FEA tools allow detecting spurious modes and select right PT shape to remove them [2]. It is important to highlight that a suitable PT design must be cleaned of spurious modes.

In addition to spurious mode removal, FEA tools provide the adequate value of electromechanical coupling coefficient (k_{eff}) as a function of the PT shape.

The main drawback of these tools is they do not provide a model to be implemented in an electrical simulator.

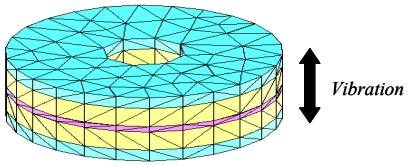


Figure 4. PT modeling by FEA tools.

Table I summarizes the features of the considered modeling alternatives. It can be concluded that the different PT analysis are not enough to fulfill modeling requirements that have been described in section II.

In this paper, a procedure to calculate parameters of 1D model based on transmission lines with the information provided by FEA tools is established. In addition, FEA tools are used to remove spurious modes. Therefore, 1D models are valid since only one-dimensional vibration is produced.

TABLE I. COMPARISON OF REQUIREMENTS OF DIFFERENT PT MODELING ALTERNATIVES

Modeling Requirements	Mason	T.Lines	FEA
Easy to implement in an electrical simulator	✓	✓	×
Analysis of the main vibration mode	✓	✓	✓
Analysis of the higher orders of main vibration mode	×	✓	✓
Analysis of spurious modes	×	×	✓
Analysis of the losses	✓	✓	✓
Analysis of fixing	×	✓	✓
Analysis of the electrode distribution	×	✓	✓
Electromechanical coupling as a function of PT shape	×	×	✓

IV. PROPOSED MODELING PROCEDURE

First of all, PT design is analyzed by 1D models. The equivalent electrical circuit model parameters for each layer, represented in figure 3.b, are given by:

$$C_o = \varepsilon_{33}^S \frac{A}{t} \tag{3}$$

$$R_{el} = \frac{1}{2 \cdot \pi \cdot f_{res} \cdot C_o \tan \delta_e} \tag{4}$$

$$k = \varepsilon_{33}^S \frac{A \cdot g_{33} \cdot c_{33}^D}{t} \tag{5}$$

$$L = \rho A \tag{6}$$

$$C = \frac{1}{A \cdot c_{33}^D} \tag{7}$$

$$R = \frac{2 \cdot \pi \cdot f_{res} \cdot L}{Q} \tag{8}$$

L and C are the transmission line inductance and capacitance per unit length respectively. R is the transmission line resistance that accounts for mechanical losses (figure 5).

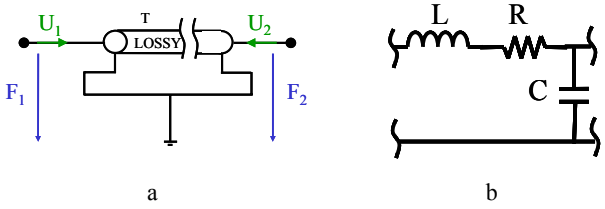


Figure 5. Equivalent circuit (b) of a transmission line (a).

The material properties required by 1D model are: the dielectric constant in the movement direction, ε_{33}^S, the piezoelectric coefficients in the movement direction (g_{33}, c_{33}^D), the material density (ρ), the mechanical quality factor (Q) and the electric loss factor ($tan\delta_e$).

The resonance frequency of PT, f_{res}, can be obtained by equation (9), where T is the total thickness of the PT design.

$$f_{res} = \frac{1}{2 \cdot T} \cdot \sqrt{\frac{c_{33}^D}{\rho}} \tag{9}$$

In addition, geometrical parameters of PT design are required. The thickness of each layer t and an equivalent electrode area, A, is needed. From the point of view of 1D model, that means that the same area is considered for a cylinder and a ring PT shape.

Therefore, the input data of PT electrical model are the material properties, which are provided by the manufacturer [13], and the geometrical dimensions of PT design.

The model for a multi-layer PT structure consists on several layers adequately connected. Figure 6 shows the connection and fixing conditions of two layers. Nodes *fin*, *fout* and *fgnd* represent mechanical connections of the layer to the previous, next and reference force nodes respectively. Nodes *vp* and *vn* stand for the electrical connections of the layer that are the electrodes.

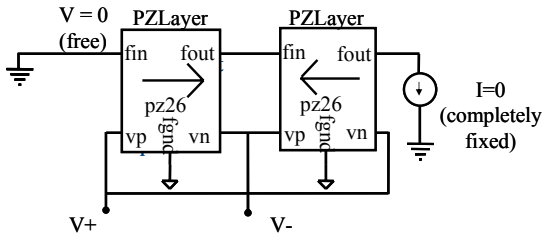


Figure 6. Layer connection and fixing conditions

Since electrical and mechanical nodes of each layer are available, different fixing conditions and layer connections can be considered. In this case one of the ends is free to move, this is modeled by means of a short-circuit indicating that there is not mechanical force reaction in this end. The

other end is completely fixed and this is modeled by means of a zero current source (open-circuit), meaning that the particle velocity in this end is zero.

At first step, it is proposed to obtain the electromechanical coupling of the multi-layer PT structure, for the main vibration mode, by considering 1D model (k_{eff_1D}). As shown in [5] the electromechanical coupling is affected by the electrode distribution.

In order to obtain the value of k_{eff_1D}, an AC analysis is running with PT in secondary open circuit conditions. From this analysis, the resonance (local minimum of the input impedance) and antiresonance frequency (local maximum of the input impedance) of PT design is obtained. The value of k_{eff_1D} is calculated by equation (2).

At second step, it is proposed a modal analysis of PT by FEA tools in order to obtain the electromechanical coupling coefficient as a function of PT shape (k_{eff_3D}) for the considered vibration mode. k_{eff_3D} can be also determined by measurements.

Finally, it is proposed to adjust the coupling between electrical and mechanical side of each layer (k), with k_{eff_1D} and k_{eff_3D} by using a very simple expression:

$$k' = k \cdot \frac{k_{eff\_3D}}{k_{eff\_1D}} \qquad (10)$$

For better understanding of this procedure, and also to validate it, a specific PT design with multi-layer structure, ring shaped and working in thickness mode has been considered.

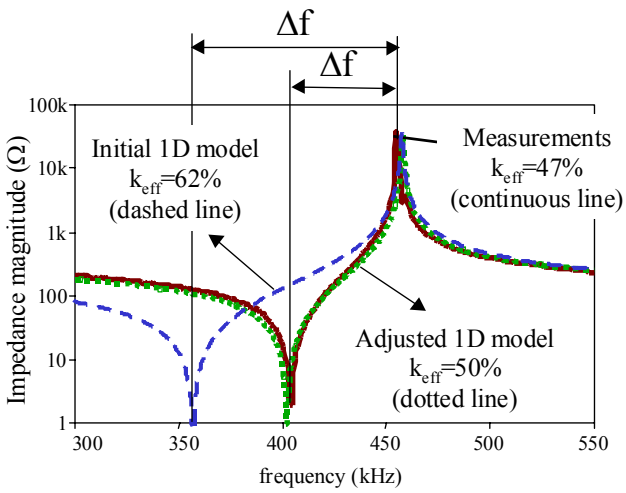


Figure 7. Input impedance magnitude with secondary open. Comparison of the initial 1D model and the adjusted 1D model with measurements

Figure 7 compares the k_{eff} value obtained with the initial model, the adjusted model and the PT sample measurements.

As seen, the initial 1D model provides the higher k_{eff} (62%) since PT shape is not taken into account. In addition, the k_{eff} value of adjusted 1D model (50%) is higher than the value obtained by measurements (47%). It is important to notice that the simulated PT does not consider electrode dimensions, electrode material and external connection of the electrodes. Hence, a reduction of k_{eff_3D} value in the PT sample is obtained compared to the predicted value by FEA tools (50%).

Therefore, the proposed modeling procedure allows obtaining the right frequency range of the converter (Δf).As mentioned in section II, the operating frequency range of the converter is located between resonance and antiresonace frequency of PT. This procedure is summarized in figure 8.

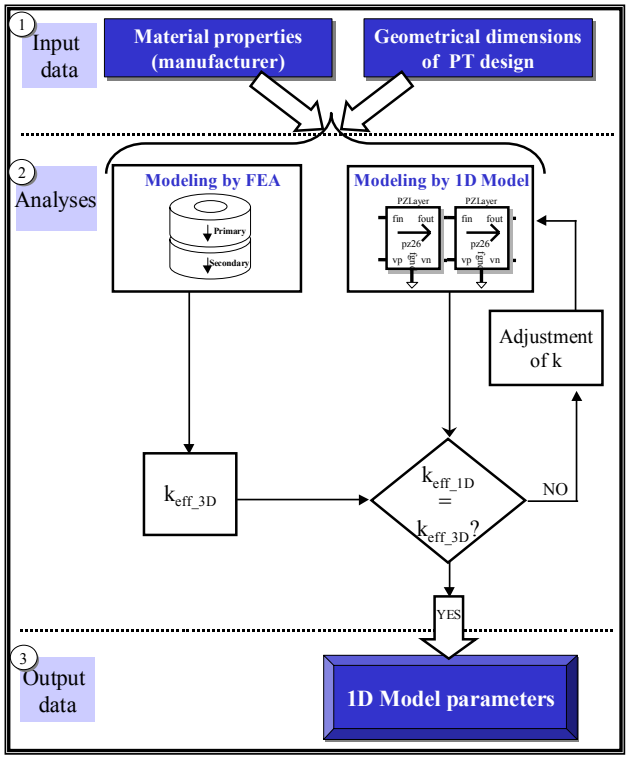


Figure 8. Proposed modeling procedure

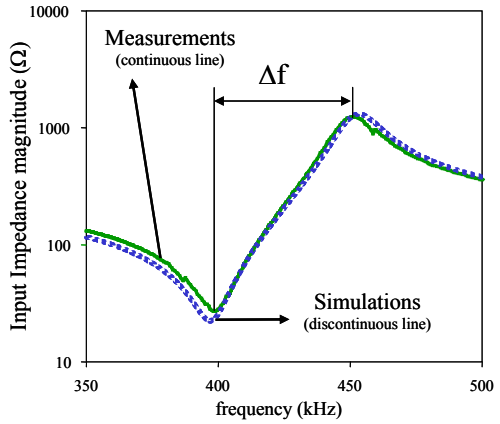
V. MODEL VALIDATION

In order to validate the features of the proposed model, a PT sample (figure 9) with multi-layer structure, ring shaped and working in thickness mode has been considered.

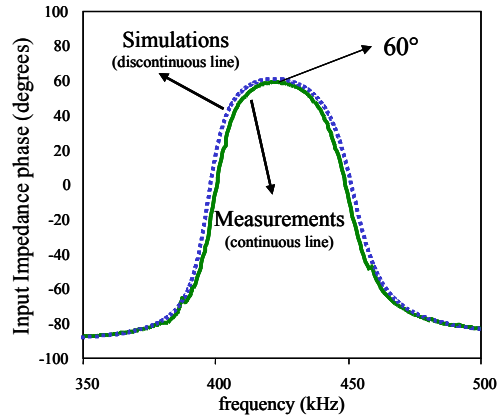
Figure 9. Picture of the considered PT sample

The obtained model has been validated not also from the point of view of the component characteristics, but also from the point of view of power converter features.

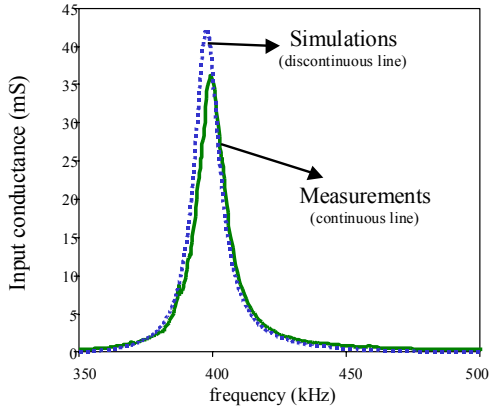
Figure 10 shows the main electrical features of PT from the point of view of power converter specifications by considering the load that provides it the maximum efficiency (optimum load). This optimum load is 5Ω.



a. Input impedance magnitude



b. Input impedance phase



c. Input conductance

Figure 10. Input impedance magnitude (a), input impedance phase (b) and input conductance (c) of the PT design with the optimum load (5 Ω). Comparison between measurements and simulations with 1D model adjusted with FEA tool information

Simulated and measured input impedance magnitude (figure 10.a) provides almost the same distance between resonance and antiresonance frequency. Therefore, the operating frequency range of the converter is adequately established.

The input impedance phase (figure 10.b) accounts for the inductive behavior needed for achieving soft switching transitions. Simulation and measurements provides similar inductive behavior, since maximum impedance phase is around 60º.

Finally, input conductance value (G) determines the transferred power (P) by the PT for a given input voltage (V_e) by the expression $P= G \cdot V_e^2$. As seen in figure 10.c maximum G is bigger (around 5mS) in simulations. However, the operating frequency range of the converter does not contain the resonance frequency due to the decrement of input impedance phase that makes soft switching transitions are not achieved.

In addition, several power tests have been realized in order to validate the proposed PT model at converter level. Figure 11 shows the power test performed by considering sinusoidal driving conditions with the optimum resistive load (R_{opt}) at secondary PT side.

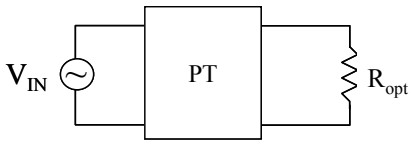
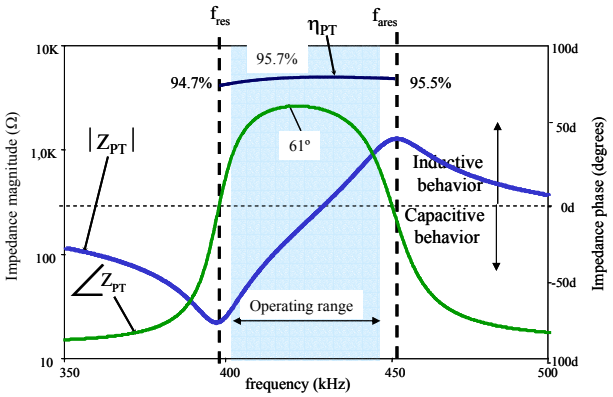
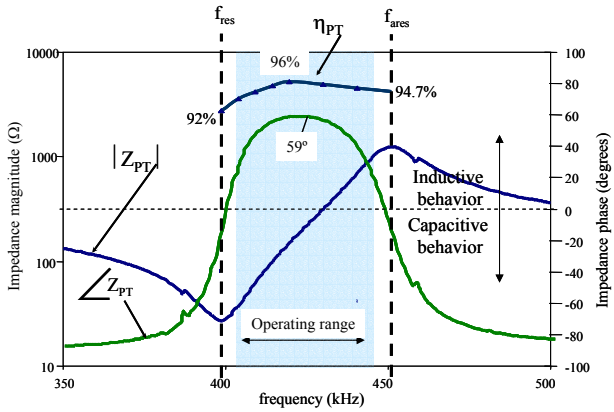


Figure 11. Sinusoidal driving power test



a. Simulations



b. Measurements

Figure 12. Input impedance magnitude ($|Z_{PT}|$) and phase ($\angle Z_{PT}$) and efficiency (η_{PT}) of PT with the optimum load. Sinusoidal driving

The most important information from sinusoidal driving is how is the efficiency versus frequency. Simulations and

measurements show that the maximum efficiency is around 96% and efficiency plot is flat between resonance and antiresonance frequency (figure 12). However there is a higher decrement of the PT efficiency close to the resonance frequency in measurements compared to simulations. Nevertheless, as mentioned before, the operating frequency range of the converter does not contain resonance and antiresonance frequency since PT input impedance phase (figure 10.b) decreases quickly close to these frequencies. Hence, it can be concluded that the obtained model is proper to design power converter since suitable PT efficiency, required inductive behavior to provide ZVS and right operating frequency range of the power converter is obtained.

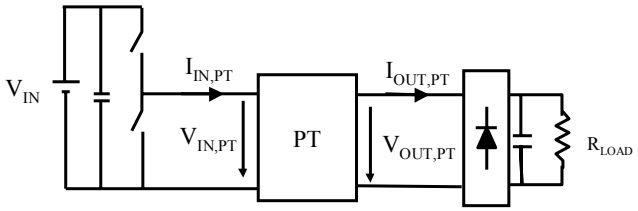
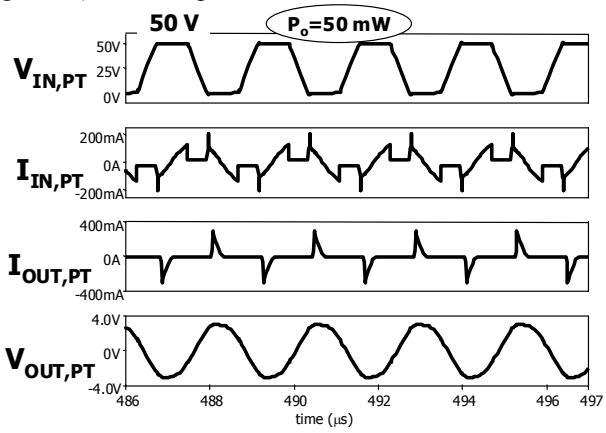
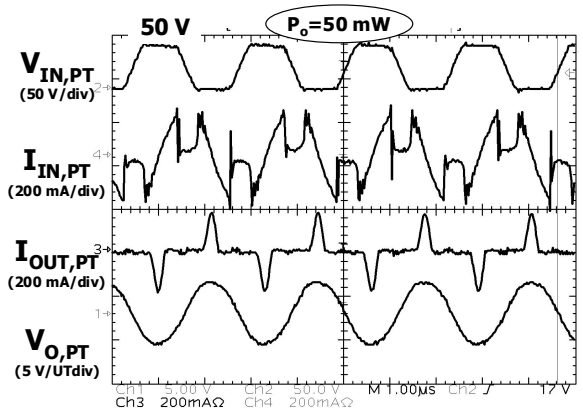


Figure 13. Power converter topology. Square driving

Finally, power test of the PT inside the power topology (figure 13) has been performed.



a. Simulations



b. Measurements

Figure 14. Input voltage ($V_{IN.PT}$), input current ($I_{IN.PT}$), output voltage ($V_{OUT.PT}$) and output current ($I_{OUT.PT}$) of PT. Square driving

As shown in figure 14, the current and the voltage at the PT input and output are very similar in simulations and measurements considering the same power level. Furthermore, PT is able to provide ZVS condition to the switches with power level close to no load condition (50mW, R_{LOAD}=180Ω) with an input voltage of 50V.

From the comparison between simulations and measurements, it can be concluded that adequately PT behavior with the proposed model has been obtained at component and at converter level.

VI. CONCLUSION

In this paper, a procedure to improve 1D model parameters, with Finite Element Analysis (FEA) information, and for multi-layer PT working in thickness mode has been proposed and validated.

This procedure requires the material properties provided by manufacturer and geometrical dimensions as input data. The information provide by FEA tools allows adjusting parameters of electrical 1D model.

This model allows designing power converter since adequate behavior of the PT is obtained at component and at converter level.

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Mixed Analytical and Numerical Design Method for Piezoelectric Transformers

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Abstract - **Analytical models are widely used for Piezoelectric Transformers (PTs) design. In this paper, the additional usefulness of Finite Element Analysis (FEA) for PT design will be shown. With FEA it is possible to optimize the PT design not only by maximizing the energy transference, but cleaning the working frequency range of spurious modes (geometrical 2D/3D effects). Besides, FEA tools allow studying other interesting aspects of the PT design such as the manufacturing tolerances or the influence of the fixing layer on the PT performance (which is a critical design point). A mixed analytical and numerical design method for PT is proposed.**

I. INTRODUCTION

Nowadays Piezoelectric Transformers (PTs) become, in some applications, an alternative to the magnetic transformers for power supplies, when the system miniaturization, high voltage conversion ratio, higher isolation voltages and low EMI content are critical design points [1-3]. In this paper, the design stages of a PT will be shown, using a specific example: a PT for an AC/DC converter of a mobile phone battery charger. The PT works in thickness mode, as it is shown in Figure 1.

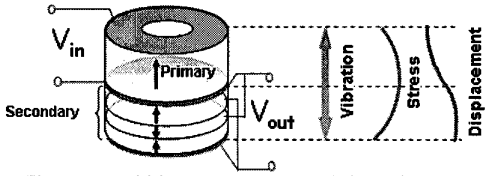

Figure 1. Multi-layer PT structure and electrodes.

Analytical equations which describe the PT behavior are difficult to solve as a 3D system [4]. So a simplification is done, considering the vibration of the PT in only one direction, the thickness direction, although displacements in other directions may exist. Resultant model is a one dimension (1D) model. With an analytical 1D model, it is possible to select the type of material, number of layers, thickness of each layer, area, interleaving of the electrodes, but not the geometry. Therefore, it is necessary to use Finite Element Analysis (FEA) tools, in order to take into account two dimension/three dimension (2D/3D) effects to select the geometry for an optimum design. The main goal in PT geometrical design is that the working frequency range (between resonance and anti-resonance) must be free of spurious modes. The spurious modes make the PT vibrate in different and non-desired directions, which implies a reduction in the PT efficiency. Apart from avoiding spurious modes, another design goal is to obtain a high electromechanical coupling coefficient (k_{eff}), in order to maximize the efficiency of the conversion and power transference, as can be deduced from the following equation:

$$\frac{Power}{Volume} \propto k_{eff}^2 \cdot \varepsilon \cdot f \qquad (1)$$

where ε is the material permittivity and f the vibration frequency.

II. DESIGN STAGES

In this section, a method for PTs design is described, combining analytical and numerical results. The method is validated with several PTs designs for the same converter specifications (universal input voltage, output voltage is 12V and output power is 10W), without loss of generality.

The power that a PT can transfer depends on the material type and area. Total thickness of the transformer is selected according with the specified working frequency. By selecting the number of layers of the primary and the secondary side of the PT, the voltage ratio is fixed [5]. All of these constructive parameters can be selected with an analytical 1D model and most of the designers stop at this stage. But it is possible to go further with FEA. This way, geometry or shape is selected in order to reduce the spurious modes at the working frequency range. Manufacturing tolerances must be taken into account in the design process because they may induce new spurious modes. Finally, as the PT is not an isolated component, it must be fixed in a PCB. As will be shown in section E, this is a very critical design point.

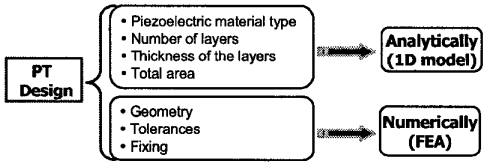

Figure 2. Design parameters of a PT

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These essential parameters for designing PTs are summarized in Figure 2. The proposed design method has been divided into five stages:

A. Topology selection

The topology is selected according to the application and converter specifications. For this particular example, a Half-Bridge inverter (Figure 3) is selected because it is widely used with PTs to generate the square voltage for this input voltage range and power level. Input AC voltage is rectified, and then DC voltage is transformed to a proper AC voltage to excite the PT (inverter stage). PT resonance frequency is inversely proportional to thickness dimension. Therefore, switching frequency is selected as a trade-off between PT thickness and switching losses. Another rectification is needed to adapt the PT output voltage (AC) to the DC voltage that must be applied to the load.

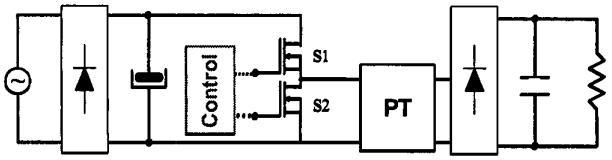


Figure 3. Converter topology

B. Analytical Modeling and Design

PT must fulfil the requirements at component and converter level. For this stage, it is very useful an analytical model [6]. This model can be easily implemented in an electrical simulator like SPICE, as it is shown in Figure 6, where the PT model is represented, and in Figure 9, where the converter circuit is also analyzed.

At component level, the design outputs are constructive parameters, such as the PT type of material, area and lateral structure of the PT (number of layers, thickness of each layer and electrode distribution). At converter level, the design outputs are electrical parameters, such as efficiency, Zero Voltage Switching (ZVS) capability, transferred power, etc.

Two 1D designs of multi-layer PTs, made of PZT material (Pz26) [7], are described and compared. They are named PT1 and PT2; its dimensions and simulation results are summarized in Table I. Transversal area of PT2 is twice PT1 one. Both of them have the same height (that is why the resonance frequencies are so similar), but these height is distributed along bulk, primary and secondary layers in a different way, as it is shown in Figure 4 and Figure 5.

Both are proper designs because efficiencies and k_{eff} are high enough. PT1 and PT2 input impedance magnitude and phase are represented in Figure 7 and Figure 8. The higher the impedance phase at the working frequency range, the easier to achieve ZVS in the whole converter [8], avoiding the magnetic components in the converter. So, it is concluded that PT2 is the best design, because it has a very good inductive behavior (PT1 maximum impedance phase is 54° and PT2 one is 77°). Although it means a penalization in PT efficiency, it keeps high enough. This result has been validated with simulations at converter level for both designs (Figure 9). Some interesting converter waveforms are shown in Figure 10 and Figure 11 for the minimum operation voltage. Two of them are PT input current and voltage waveforms, which are useful to test ZVS capability. It has not been possible to achieve ZVS with PT1; nevertheless PT2 has ZVS in the whole voltage range.

TABLE I
PTS FEATURES.

	PT1	PT2
Area	100 mm^2	200 mm^2
Height	4.1 mm	4.1 mm
Primary	2 layers x 0.7mm	2 layers x 1mm
Secondary	4 layers x 0.1mm	2 layers x 0.1mm
Bulk	2 layers x 1.15mm	2 layers x 0.95mm
f_{res}	502 kHz	490 kHz
k_{eff}	43%	47%
Efficiency	96%	93%

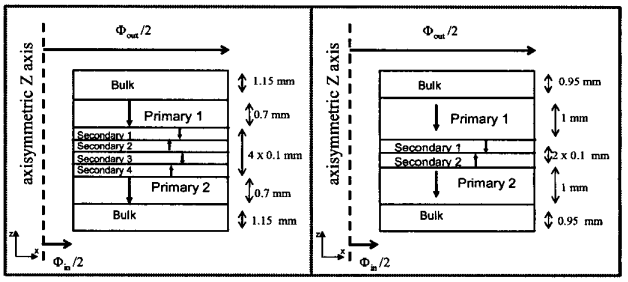


Figure 4. Axial view of PT1 ring

Figure 5. Axial view of PT2 ring

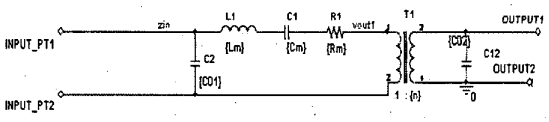


Figure 6. Equivalent circuit of a PT.

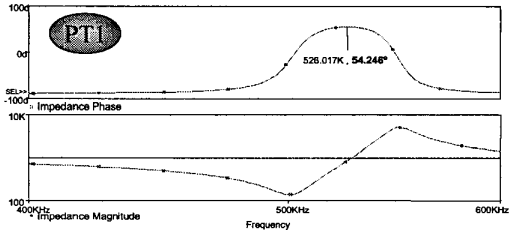


Figure 7. PT1 small signal waveforms.

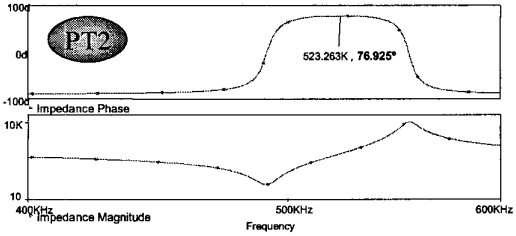


Figure 8. PT2 small signal waveforms.

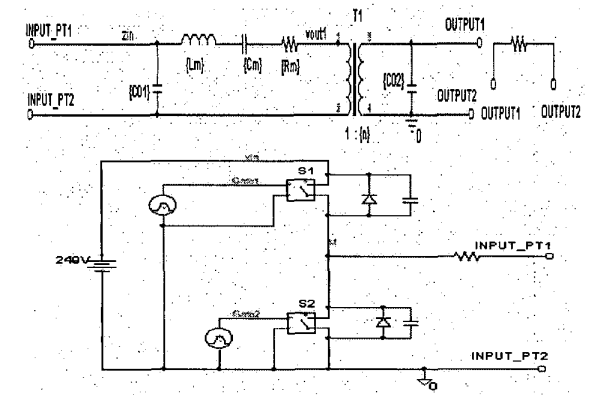


Figure 9. Global converter schematic.

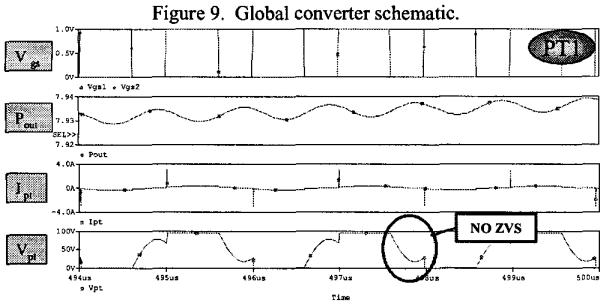


Figure 10. PT1 converter waveforms. Gate-source voltages (V_{gs}), output power (P_{out}), PT1 input current (I_{pt}) and PT1 input voltage (V_{pt}).

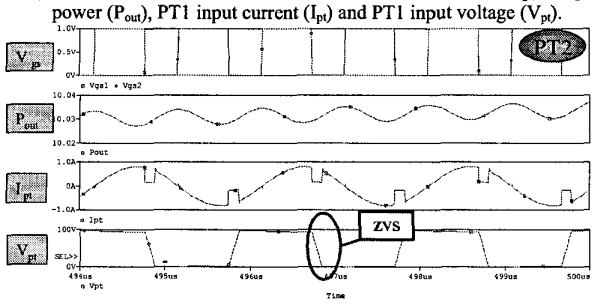


Figure 11. PT2 converter waveforms. Gate-source voltages (V_{gs}), output power (P_{out}), PT1 input current (I_{pt}) and PT1 input voltage (V_{pt}).

C. 2D/3D Design. Geometry Selection

With 1D analysis, it can be determined the thickness of each layer and the total area. But there are a lot of geometric possibilities for the PT dimensioning, such as a disc, ring, plate, etc. FEA tools are useful to distribute the area in a correct geometry, that is to implement the 1D design in a proper 3D design. So, as an example of 2D/3D design, a ring shape for PT2 is selected, similar to the one of Figure 23. The aim is to show how critical can be the selection of the internal and external diameters (ϕ_{in} and ϕ_{out}) of the ring, keeping the area as a constant. Interleaving of electrodes (which consists on placing the secondary electrodes between the primary ones) is used in order to improve the PT electrical performance, as it is explained in [9].

FEA tool selected is ATILA® [10], because it is specially developed for the simulation of the electromechanical coupling in 2D/3D of piezoelectric materials. As it was seen in Figure 5, PT ring presents axial symmetry (being z the symmetry axis). Therefore, 2D and not 3D analyses are done in order to reduce the computing time, since no important different results are obtained, as will be analyzed later.

The result of a modal analysis with FEA tool is k_{eff} as a function of frequency. So, modal analyses have been made for two different diameters selection: PT2a with ϕ_{out}=19.73mm and ϕ_{in}=11.61mm and PT2b with ϕ_{out}=24.97mm and ϕ_{in}=19.21mm. It is very useful because it allows to test whether the working frequency range is free of spurious modes or the k_{eff} of thickness mode is high enough (around 40%), because k_{eff} depends not only on the material properties but on the specific geometry.

As shown in Figure 12, diameters in PT2a are not appropriate, since there are many spurious modes close to the resonance frequency. On the contrary, for PT2b the selection of diameters is right because the working frequency range is clean of spurious modes (Figure 13). Besides PT2b k_{eff} is higher than PT2a k_{eff}, due to the reduction of the spurious modes close to the resonance. It is necessary to emphasize that finding the correct diameter is not an easy task: for the same area, more than five combinations of ϕ_{out} and ϕ_{in} have been analyzed and only one, PT2b, fulfils the requirements.

Other useful information from FEA is electric field and stress distribution, which limits the PT power density [11]. It is also possible to extract graphics of the displacement for each frequency, which is suitable to understand the PTs mechanical behavior. It is shown in Figure 14 that PT2b vibration between resonance and anti-resonance frequency consists on a compression and expansion along PT thickness (Z axis), that is the first order of thickness mode.

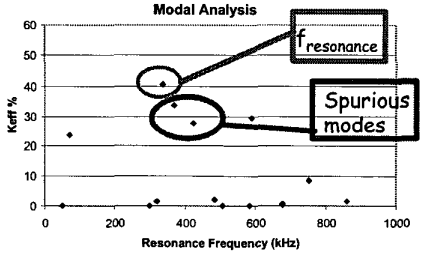


Figure 12. k_{eff} vs resonance frequency. PT2a design.

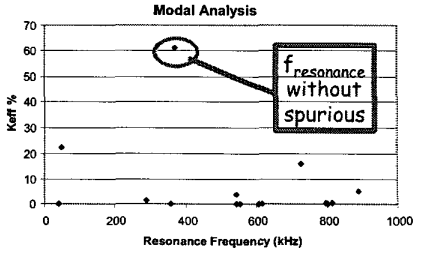


Figure 13. k_{eff} vs resonance frequency. PT2b design.

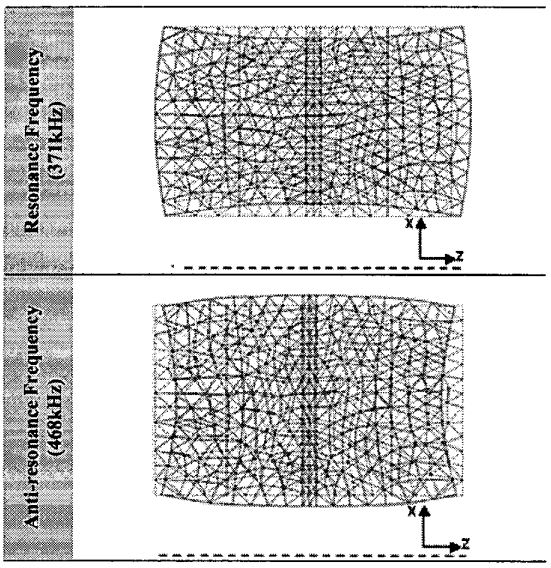


Figure 14. Axial View of the PT2b vibration in thickness mode. Discontinuous line represents the initial structure, without deformation and continuous line represents the deformed structure by applying a voltage to the primary side.

FEA results have been validated with measurements in real samples. If the selection of diameters is bad, the PT input impedance for the open circuit condition presents spurious modes (Figure 15). But if the selection of diameters is right the input impedance is free of spurious modes (Figure 16).

All the previous PTs designs have a symmetry axis, so 2D analyses can be developed. 3D analyses have no symmetry restrictions in the structure to analyze but the time to define and solve the problem is longer than in a 2D analysis. 3D study has the advantage of being the most accurate. Therefore a 3D harmonic analysis of the PT2b has been done to be compared with the 2D one. The main result of the harmonic analysis is a graph of impedance as a function of the selected frequencies, as it is shown in Figure 17.

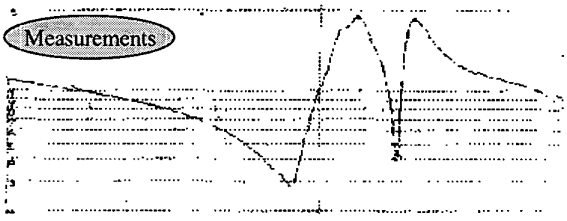


Figure 15. Input impedance vs frequency. Bad PT design.

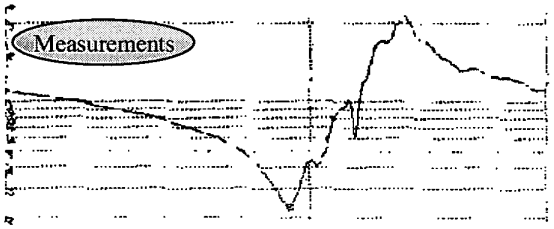


Figure 16. Input impedance vs frequency. Good PT design.

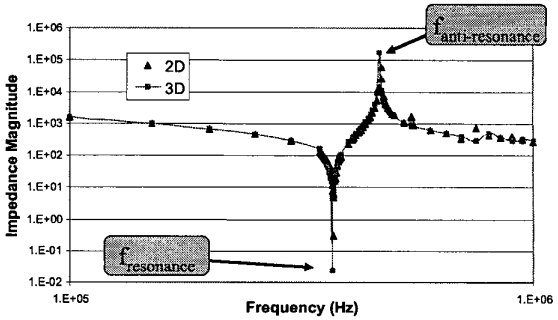


Figure 17. Input impedance vs frequency. Comparison between PT2b 2D and 3D results.

It is deduced from Figure 17, that 2D and 3D impedance curves are very similar. However, maximum and minimum impedance values are more accurate in a 3D analysis. Regarding the solving time, it goes from a few minutes in 2D to several hours in 3D analysis, using a Pentium IV with 256MB of RAM.

Therefore, 2D or 3D analyses will be chosen depending on the specific design requirements. In general, it is advisable to take advantage of the symmetries to simplify the problem.

D. Manufacturing Tolerances Influence on the PT Performance

PT working frequency range must not be sensitive to dimension changes caused by the manufacturing tolerances. The manufacturing of Pz26 material presents tolerances about ±3% for the thickness of each layer, ϕ_{in} and ϕ_{out}. Several combinations of tolerances have been tested for the PT2b design; some of them have influence and other not. For example, considering a tolerance of -3% in thickness and ϕ_{in} and +3% in ϕ_{out}, there is a reduction in k_{eff}, comparing with the nominal case, and also a spurious mode appears close to the resonance (Figure 18).

An optimum design must not be sensitive to these tolerances. In addition to that, it would be necessary to warn the PT manufacturer about the critical dimensions.

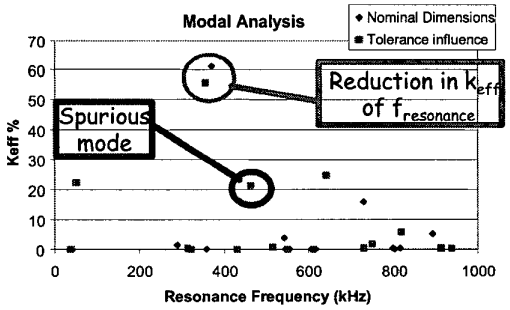


Figure 18. k_{eff} vs resonance frequency. Tolerances influence on PT2b.

E. Fixing Layer Influence on the PT Performance

Fixing the PT to the PCB is a difficult point, because the vibration of the PT can be perturbed, modifying its electrical performance. Fixing can also be used to provide a path for thermal dissipation. Anyway, it is necessary that the fixing method ensures the mechanical robustness of the converter. Three different ways have been tested:

- With a thermal glue at the bottom part. It is very simple but the drawback is that efficiency drops dramatically, because PT natural vibration is not allowed.

- Using clips or screws. This method keeps efficiency almost constant, especially if a thermally conductive foam is also used for fixing [12]. But, in this particular case, it is not easy to access to the electrodes for soldering the wires.

- Adding a fixing layer, as a belt, to the PT. This fixing method is the one selected because it makes easier the connection to the PCB with thermal glue and the soldering of wires (if the electrodes are placed in the fixing belt). It also has the advantage of providing a thermal path. The main drawback is that it is very sensitive to the spurious modes. So, FEA modal analyses are mandatory in the fixing belt design.

PT2b design is selected in order to study the fixing layer influence. Vibration figures with the fixing layer free and glued are grouped in Table II. If the fixing layer is left free a spurious mode appears near the anti-resonance frequency, inducing a wrong movement, and the k_{eff} is reduced too (Figure 19). But these problems disappear if the fixing belt is glued, because PT vibrates in thickness mode and the resonance frequency has no spurious in its vicinity (Figure 20), as it was desired.

It is also interesting to study the effect on the PT of the fixing layer position. FEA result of PT with glued central fixing layer has been compared with the result of the fixing layer moved to a lateral position (Figure 21).

With the lateral fixing layer a new spurious mode appears near the resonance frequency (Figure 22). This justifies why, in general, the fixing layer must be placed in the area of minimum displacement (near the node points), which for this specific design is placed in the middle of its thickness (Figure 1).

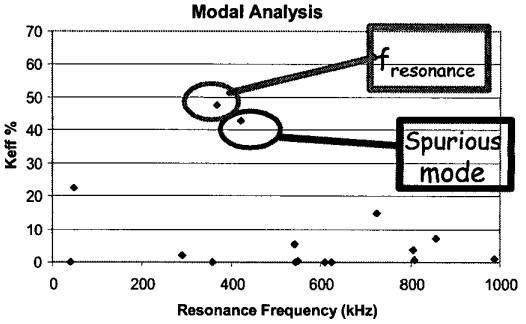


Figure 19. k_{eff} vs resonance frequency. Free central fixing layer.

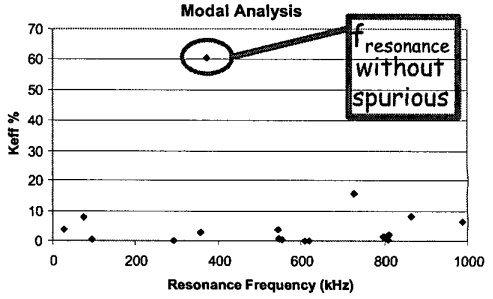
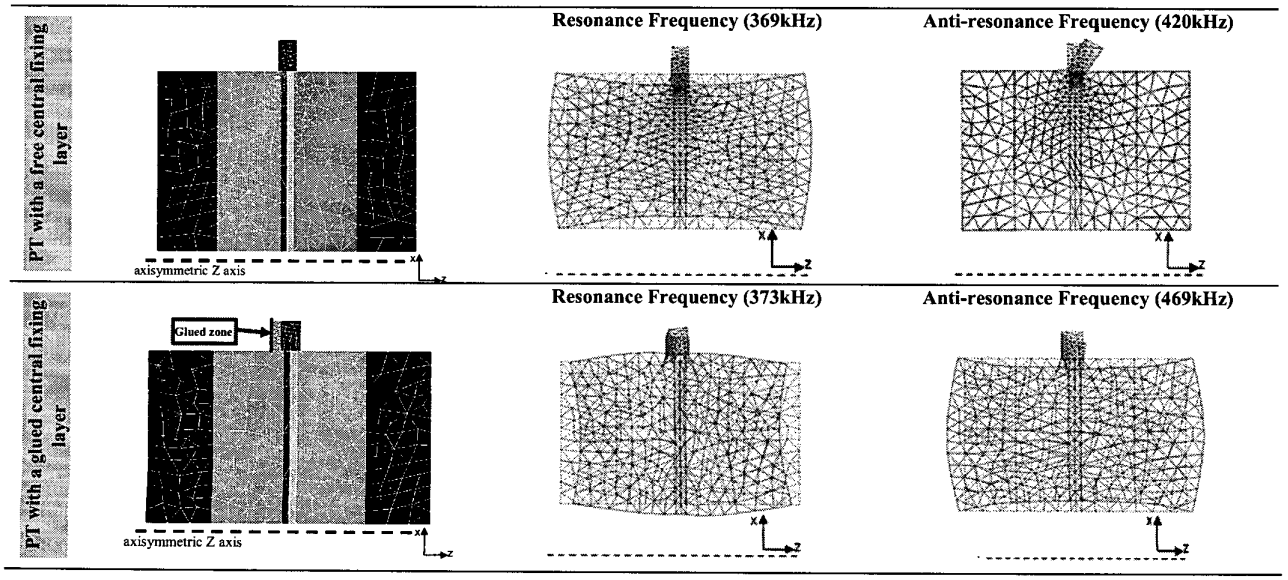


Figure 20. k_{eff} vs resonance frequency. Glued central fixing layer.

TABLE II

AXIAL VIEW OF THE PT VIBRATION AT THE RESONANCE AND ANTI-RESONANCE FREQUENCIES.



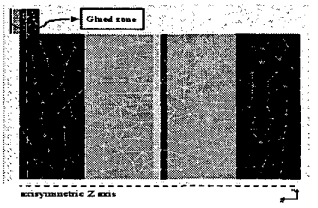


Figure 21. PT ATILA mesh with a glued lateral fixing layer.

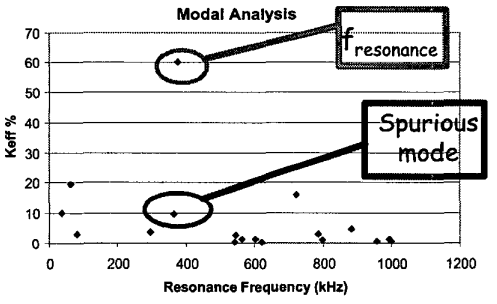


Figure 22. k_{eff} vs resonance frequency. Glued lateral fixing layer.

Finally, a 3D view of the PT2b design with the proper fixing layer is presented in Figure 23.

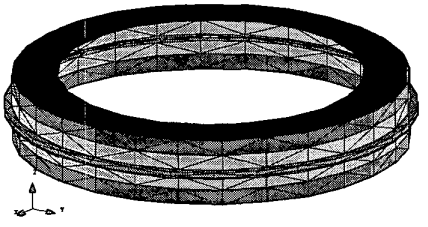


Figure 23. 3D view of the designed PT.

III. CONCLUSIONS

In this paper, a design method for PT has been proposed and validated. This procedure consists on a combination of analytical and numerical design. It takes into account not only 1D effects (with analytical models), but 2D/3D effects (with FEA tools). Shape, tolerances and fixing of the PT are the main 2D/3D effects that must not be forgotten in the design process. It consists of the following stages:

- Topology selection
- Analytical Modeling and Design
- 2D/3D Design. Geometry Selection
- Manufacturing Tolerances Influence on the PT Performance
- Fixing Layer Influence on the PT Performance

Since PTs design is a complex task, this method makes possible an optimization before manufacturing it, reducing the time and cost of the process.

The method has been successfully applied to several examples of PTs design, with good results both at component and converter level. This design method is also useful to achieve ZVS, suppressing the inductor of the converter. Inductor increases significantly the total volume of the converter, as can be seen in Figure 24 [13]. Both PT and inductor have a similar size, when PT has not been designed to achieve ZVS. It is pending to build the magnetic-less converter with PT2b to validate its performance.

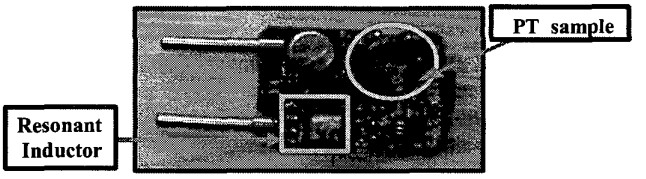


Figure 24. Photograph of the power converter. PT and magnetic component are highlighted

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Step by Step Multi-layer Piezoelectric Transformer Design Procedure

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Abstract— Piezoelectric Transformers (PTs) provide several advantages compared to magnetic components that are higher power density, lower radiated noise and higher voltage isolation capability. PT must be properly designed to benefit the power converter with the advantages aforementioned. In this paper, a step by step procedure to determine the electrode area, the type of material, the number and thickness of the layers and the electrode distribution considering power topology restrictions is presented.

I. INTRODUCTION

Higher power densities, lower radiated noise and higher voltage isolation capability of Piezoelectric Transformers (PTs) compared to magnetic transformers make PTs attractive for low power applications, where these features are critical issues [1] – [5].

The general procedure to design a PT for an application has been established in [6]. The different stages of this procedure are: topology selection, analytical design, geometry selection, manufacturing tolerances analysis and fixing design.

This paper is focused in the second stage: analytical design of a PT.

In order to validate the proposed design procedure an AC adapter for mobile phone with universal input voltage range (85Vrms-265Vrms), 8.4 W of output power and 12 V of output voltage, has been selected. Since the AC adapters for mobile phones should be as small as possible, PTs are a good candidate to achieve this goal.

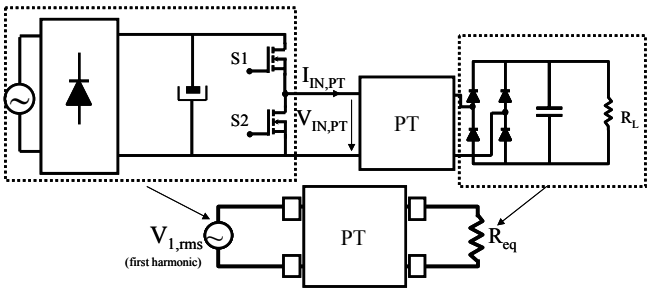

Figure 1. Considered power converter topology (magnetic-less) and its equivalent system

For this particular example, a Half-Bridge inverter (figure 1) is selected in terms of the required input voltage range and power level. Input AC voltage is rectified, and then DC voltage is transformed to a proper AC voltage to drive the PT (inverter stage). Another rectification is needed to adapt the PT output voltage (AC) to the DC voltage that must be applied to the load (R_L). Full bridge rectifier has been selected because no magnetic components are needed.

Once power converter topology has been chosen, the next stage is the analytical design of the PT. At this stage, electrical models, that only consider the main vibration mode (1D) are employed to determine the degrees of freedom of PT in order to obtain the electrical PT features required by the application.

PT working in thickness mode (figure 2) has been selected to obtain a low profile converter. In addition, multi-layer PT structures are needed to obtain the low output impedance (around 17 Ω) required by the selected application.

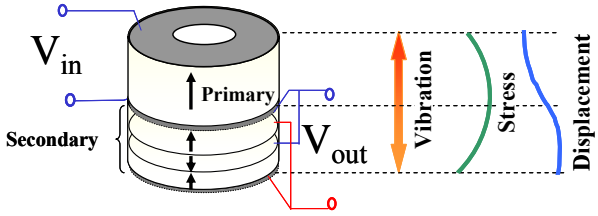

Figure 2. Multi-layer PT working in thickness mode

In this paper, a design procedure to determine the different degrees of freedom of PT (material, area, thickness number and position of layers) is presented.

It is important to highlight that PT design is realized by taking into account power converter topology restrictions in order to benefit the application with the PT advantages, avoiding the use of magnetic components.

II. ELECTRICAL PT REQUIREMENTS

Most designers use Mason model because it is simple and provides an analytical relation between geometric parameters and electrical properties of the PT. However, obtaining mason model parameters for the required multi-layer structures is not an easy task. Hence, model based on transmission lines has been selected. The features of this model have been detailed in [7].

As described in [8], the required electrical specifications of the PT can be obtained analyzing the equivalent system of the power converter topology shown in figure 1.

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This equivalent system substitutes the inverter stage of the topology by a sinusoidal voltage corresponding to the first harmonic of the square voltage at the output of the Half- Bridge inverter ($V_{1,rms}$). In addition, output stage of the converter (rectifier and load) can be substitute by an equivalent resistive load (R_{eq}). The value of R_{eq} depends on the type of rectifier stage [3]. Full wave rectifier provides higher R_{eq} than half wave rectifier. As analyzed in [9] lower PT size (lower area) and cost (lower number of secondary electrodes) is achieved by using full wave rectifier.

The electrical requirements of the PT to transfer the power of the application to the considered load are the input conductance and the equivalent resistive load seen by the PT. In addition, driving voltage waveform must be taken into account. Although square driving penalizes PT performance, it allows improving PT converter since magnetic components are avoided. Therefore, higher vibrations orders and soft switching condition must be taken into account.

These electrical requirements are detailed below.

A. *Input conductance (G_{PT})*

Since PT efficiency (η_{PT}) is almost constant in the operating frequency range, output power of the PT ($P_{o,PT}$) can be expressed in terms of G_{PT} and the first harmonic ($V_{1,rms}$) of the input voltage: $P_{o,PT} = G_{PT} \cdot V_{1,rms}^2 \cdot \eta_{PT}$. An estimation of PT plus rectifier efficiency is required in order to obtain G_{PT} in terms of output power (P_o).

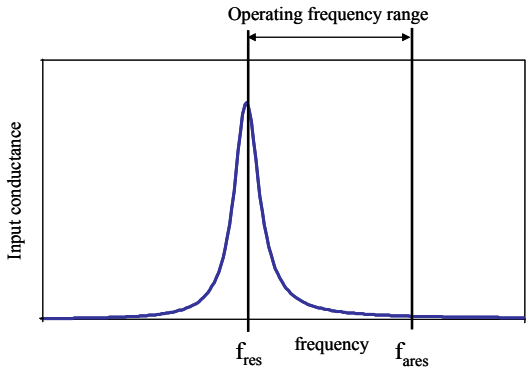


Figure 3. Input conductance (G_{PT}) as a function of the frequency and a resistive load in secondary side

The value of **G_{PT}** depends on the frequency and the resistive load seen by the PT. Therefore, this electrical parameter **accounts for input voltage and load regulation of the converter by varying the switching frequency**.

In the example, the required G_{PT} varies from 0.33mS and 3.2mS to obtain the input voltage variation ($85V_{rms}$ to $265V_{rms}$) and the power level (8.4) by considering 50% of duty cycle and PT and rectifier efficiency of 88%. This efficiency value is reasonable from the point of view of power converter efficiency [5].

B. *Equivalent resistive load (R_{eq})*

The load that implies the maximum PT efficiency is defined as the optimum load (R_{opt}). **The optimum load of the PT should correspond to the R_{eq} seen by the PT when it is transferring the maximum power**. For the selected application, output load is 17Ω and the equivalent value is 14Ω with a full wave rectifier ($R_{eq}=(8/\pi^2)\cdot R_L$).

C. *Harmonic removal*

Since PT is driven with square voltage that contains harmonics of several orders, PT design should minimize the magnitude of higher orders of the main vibration mode (figure 4) . If the high order harmonics of the input voltage are excited, PT performance worsens because it vibrates in different directions.

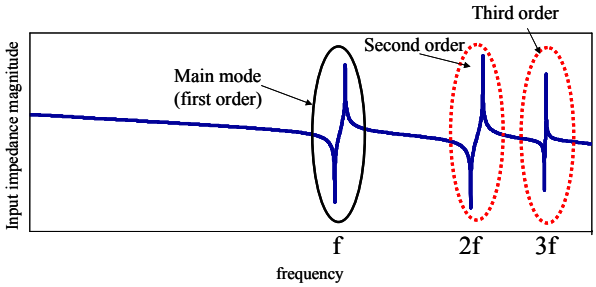


Figure 4. Input impedance magnitude versus frequency

The symmetry of the primary electrodes related to the stress distribution allows avoiding high order harmonics (figure 5). Second harmonic is avoided by using interleaving of the electrodes [10] and **third harmonic is avoided by placing primary electrodes symmetrically** related to the stress distribution of the third vibration order of the main mode.

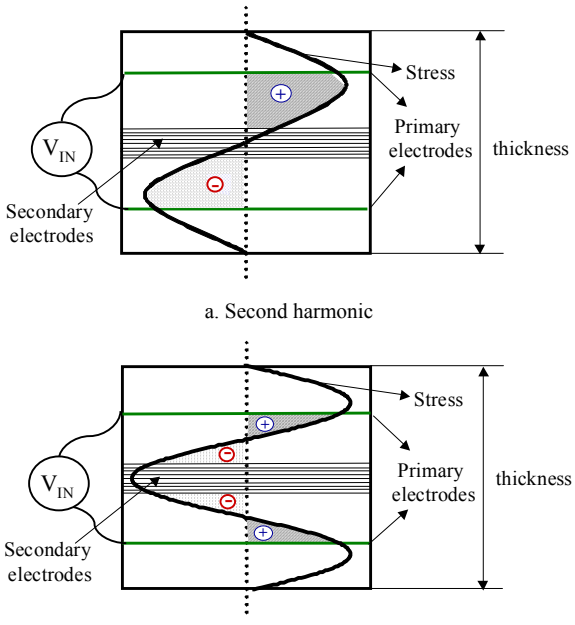


Figure 5. Removal of second (a) and third (b) harmonic of the input voltage (V_{IN})

D. *Soft switching voltage transitions (ZVS)*

Soft voltage transitions at the PT input are needed to have good performance of the PT [11]. Although PT design for ZVS condition penalizes PT efficiency and size, it makes

possible to eliminate the additional magnetic elements (impedance matching) required to achieve ZVS condition.

In addition, ZVS condition becomes critical in order to reduce the switching losses and to increase the converter efficiency since Half-Bridge inverter is operating at high frequencies. **Design PT with good inductive behavior** (figure 6) **allows PT to provide ZVS.**

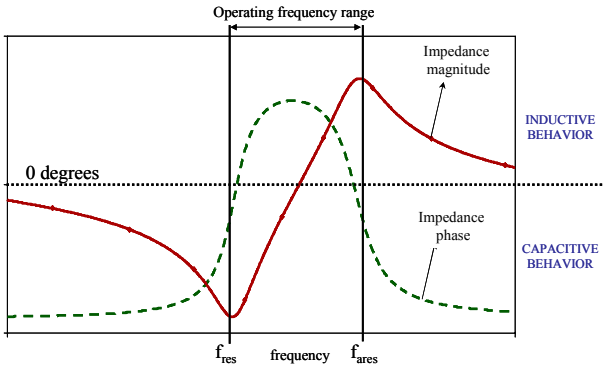


Figure 6. Input impedance magnitude and phase versus frequency

III. PROPOSED PT DESIGN PROCEDURE

The selection of the constructive parameters of the PT must be realized by:

- **Obtaining maximum electromechanical coupling coefficient (k_{eff}).**

  Equation (1) shows how power density (Power/Volume) depends strongly on this parameter. ε is the material permittivity and f is the vibration frequency.

$$\text{Power}/\text{Volume} \propto k_{eff}^2 \cdot \varepsilon \cdot f \qquad (1)$$

- **Accounting for the limitations in the PT performance** due to material properties [12]. These limitations are: maximum stress, maximum strain, maximum electric field, maximum electric displacement and maximum temperature rise.

Since there is no analytical relation between electrical parameters and constructive parameters, sensitivity analysis is required in order to obtain design rules of the PT.

Using these design rules, it is easy to change the physical PT structure to meet the electrical specifications of the PT.

The described electrical features can be obtained selecting the suitable values of the area, the number of layers, the thickness of the layers and the position of these layers.

Table I summarizes the results from sensitivity analysis that have been performed in [9]. **From this sensitivity analysis, design rules** for step-down applications and the considered PT structure **are obtained**.

For the selected application, the design criteria of PT are lowest size (lowest area) and cost (lowest number of the electrodes). That means, the thickness of secondary layers has been reduced to obtain the low value of equivalent resistive load (R_{eq}) and primary layer thickness has been increased to achieve ZVS.

Once it is known how constructive parameters affects electrical characteristics, the design steps to obtain the electrical characteristics define in section II are defined below.

- **STEP 1: Selection of the material**

  PZT material type has been selected due to the high value of permittivity (ε) since higher power density can be achieved (Power/Volume $\propto \varepsilon \cdot k_{eff}^2 \cdot f$). In this particular example, the high input voltage value requires a material with low dielectric losses. Therefore, PZ26 has been selected [13].

- **STEP 2: Selection of the PT thickness**

  The operating frequency range of the converter is fixed by the PT in the frequency range where is able to transfer energy efficiently and provide ZVS condition (between resonance and antiresonance frequency). The PT resonance frequency (f_{res}) is inversely proportional to the thickness dimension of the device, as it is shown in equation (2), where ρ and c_{33}^D are material properties.

$$\text{Thickness} = \frac{1}{2 \cdot f_{res}} \cdot \sqrt{\frac{c_{33}^D}{\rho}} \qquad (2)$$

Hence, the higher the frequency the lower the PT size. Nevertheless, the higher the frequency the higher the switching losses of the converter. Therefore, **the optimum switching frequency is a trade-off between the PT size and the switching losses.**

In this particular case, this analysis has not been realized and the minimum possible frequency due to manufacturing restrictions (maximum thickness is 4mm) has been selected in order to reduce switching losses. Taking into account equation (2), resonance frequency of the PT is around 400kHz. This frequency is a good trade-off between size and efficiency.

TABLE I.
INFLUENCE OF THE PT CONSTRUCTIVE PARAMETERS IN THE PT ELECTRICAL PROPERTIES

Constructive parameter	R_{opt}	Maximum G_{PT}	η_{PT}	k_{eff}	ZVS
↑ Area	Decrease	Increase	Constant	Constant	Improve
↑ Number of secondary layers	Decrease	Constant	Constant	Constant	Worsen
↑ Thickness of secondary layers	Increase	Decrease	Constant	Constant	Constant
↑ Thickness of primary layers	Constant	Decrease	Constant	Has an optimum value	Improve
↑ Number of primary layers	Constant	Increase	Constant	Constant	Improve
↑ Thickness of isolation layer	Decrease	Constant	Decrease	Decrease	--

- **STEP 3: Selection of the minimum electrode area**

Maximum PT temperature is determined by Curie point where piezoelectric material loses its properties. Maximum losses require a minimum PT volume to limit the PT temperature rise (ΔT).

Since PT thickness is fixed by switching frequency, the **minimum electrode area is determined by the maximum ΔT**.

The peripheral area of the PT (A) can been established in terms of its efficiency (η_{PT}) and output power ($P_{o,PT}$) by equation (3), where h (15W/m^2·°C) is the convection coefficient.

$$\Delta T = \frac{1}{h \cdot A}\left(\frac{1}{\eta_{PT}} - 1\right) \cdot P_{o,PT} \qquad (3)$$

Regarding previous experience [5], a PT efficiency of 98% and a temperature rise of 55º are determined. By taking into account equation (3), the minimum electrode area is 60mm^2.

- **STEP 4: Selection of the electrode distribution**

The different electrodes distributions have been analyzed in [10]. Interleaving of the electrodes provides higher values of k_{eff} and removes odd harmonics as was detailed in section II.

Interleaving of electrodes that consists on placed the secondary electrodes between primary electrodes has been selected since it allows higher separation of primary electrodes required for the high input voltage of the application. In addition, it allows avoiding insulation layer increasing η_{PT} and k_{eff} values.

- **STEP 5: Selection of the thickness and number of secondary layers**

Number and thickness of secondary layers are selected in order to obtain the required resistive load (14Ω).

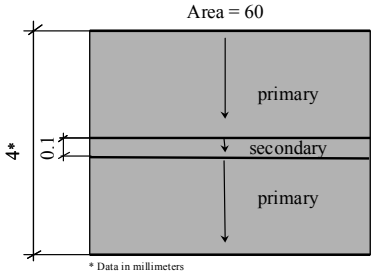


Figure 7. Initial PT structure

From sensitivity analysis, the minimum thickness of the secondary layers has been chosen. The minimum thickness of secondary layers is determined by the most restrictive condition between manufacturing limit (100μm) and maximum electric field (2kV/mm). Since secondary side has low voltage level (12V), manufacturing limit is the most restrictive one. Therefore, the initial structure that must be analyzed is shown in figure 7.

Since this structure has a 106 Ω optimum load, an increment of the number of secondary layers is required. Therefore, eight layers of 100 μm (figure 8) are required to obtain the value of R_{eq}. In addition, the efficiency of the PT (98.4%) and k_{eff} (56%) are high.

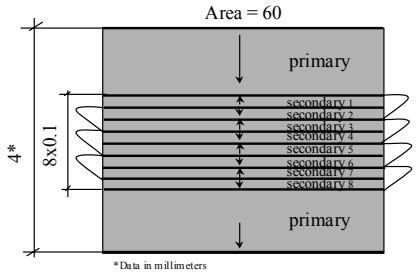


Figure 8. Adjustment of R_{eq} by selecting the number and thickness of secondary layers

- **STEP 6: Selection of the thickness and number of primary layers. Addition of bulks**

The G_{PT} value of the designed PT (figure 8) is 1.35mS that is lower than the specified, 3.2mS. **The thickness of primary has been reduced to increase the G_{PT}** instead of increasing primary layers or the area since lower cost and size is obtained. No poled layers, named as bulk layers, have been added to keep constant the PT thickness. In addition, **bulk thickness is selected to remove third harmonic** as explained in section II.

Maximum input PT voltage applied to the PT is 373V. Therefore, minimum primary thickness of 187μm can be used due to maximum electrical field (2kV/mm).

In this case, 0.5mm of primary layer and 1.1mm of each bulk zone is required (figure 9) to fulfill both requirements (maximum G_{PT} and third harmonic removal). This design provides high efficiency of the PT (98.4%) and high k_{eff} (53%).

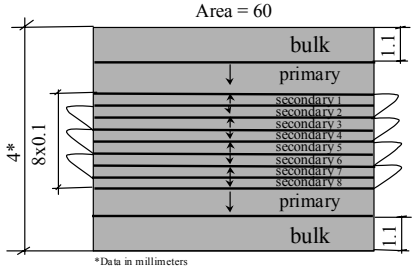


Figure 9. Adjustment of G_{TP} and third harmonic removal by selecting the number and thickness of primary layers and the thickness of bulk layers. PT1 design

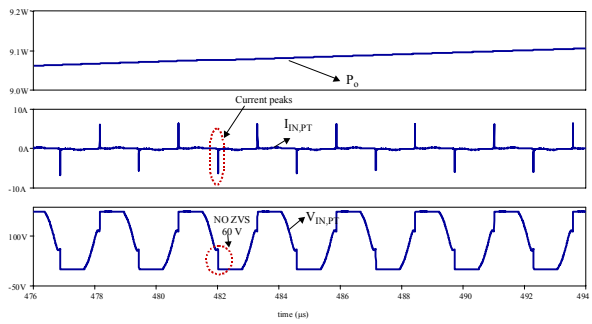


Figure 10. Analysis of zero voltage switching condition considering PT1 design

The last electrical requirement is the achievement of soft switching transitions in the input voltage of the PT. figure 10 shows that the designed PT (figure 9) is not able to provide ZVS. Taking into account sensitivity analysis (Table I), an increment of the number of primary layers is suitable in order to improve the ZVS behaviour of the PT without increasing its size.

Nevertheless, the minimum thickness and also the maximum number of primary layers are limited by maximum electrical field since the high input voltage produces high dielectric losses.

Mason model of the PT, represented in figure 11, has been used to explain this PT performance limitation.

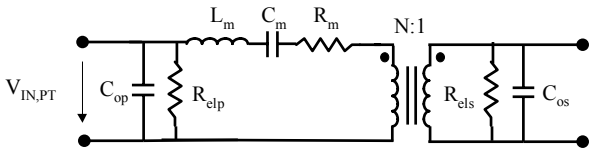


Figure 11. Mason model of a PT

Losses in piezoelectric materials have two different origins, mechanical and dielectric. Mechanical losses are modeled by the resistor R_m and dielectric losses are modeled by a resistor (R_{elp} and R_{els}) in parallel with the capacitance of primary (C_{op}) and secondary (C_{os}) PT side respectively [7].

The value of the resistor depends on the parallel capacitance as it is shown in equation (4), where $\tan\delta_e$ is a material property.

$$R_{el} = \frac{1}{\omega C_o \tan\delta_e} \quad (4)$$

Therefore, dielectric losses of PT (L_d) can be evaluated in terms of the rms value of applied voltage (V_{ms}) by equation (5):

$$L_d = \frac{V_{rms}^2}{R_{el}} \quad (5)$$

Since high PT input voltage ($V_{IN,PT}$) values are required, primary dielectric losses must be limited under the maximum PT losses. Therefore, a minimum R_{el} value or maximum C_{op} value is obtained.

The lower the primary thickness and the higher the number of primary layers, the bigger the C_{op} value. Therefore, minimum primary thickness and maximum number of primary layers is required.

Taking into account this limit, an increment of the primary layers is not possible. Therefore, it is necessary to reduce the number of secondary layers. Due to the influence of the geometric parameters in several electrical PT features (Table I), it is necessary to come back to step 5 to obtain the optimum design. PT size is penalized by increasing the area in order to achieve the value of R_{eq}.

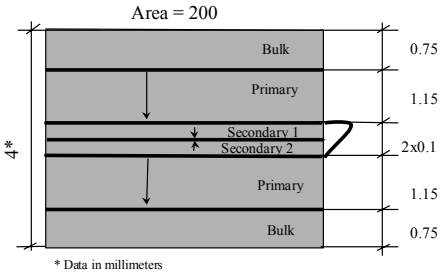


Figure 12. Adjustment of ZVS condition. PT2 design

Finally, a PT design (figure 12) with only two layers in secondary side but an area of 200 mm^2 allows to achieve all the electrical requirements (figure 13):

- G_{PT} values since the maximum value is 31.9mS.
- R_{eq} value:14Ω.
- Third harmonic removal (figure 14).
- Good inductive behavior to provide soft switching transitions. The maximum impedance phase is 76º.

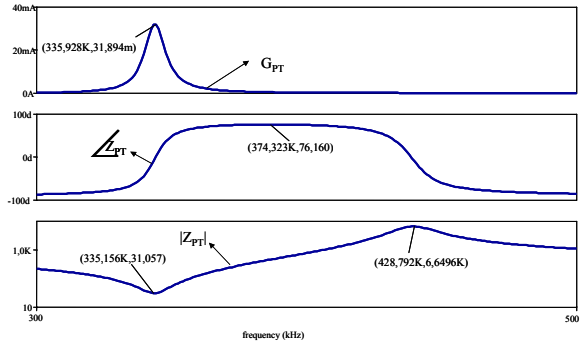


Figure 13. Input impedance magnitude ($|Z_{PT}|$) and phase ($\angle Z_{PT}$) and input conductance (G_{PT}) of PT2 design with its optimum load (14 Ω)

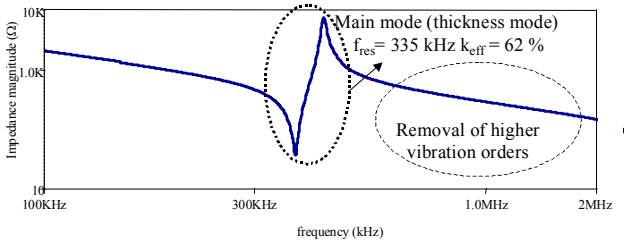
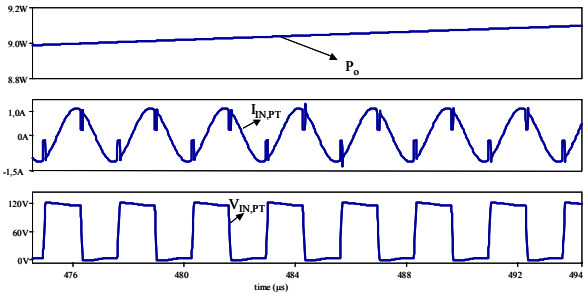


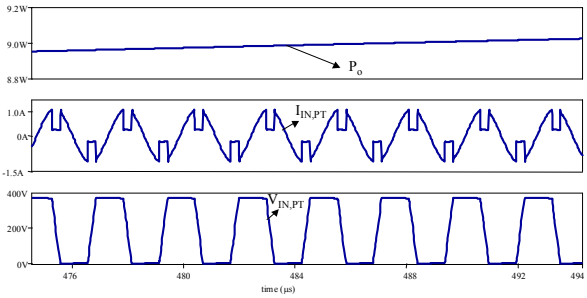
Figure 14. Input impedance magnitude of PT2 design with its optimum load (14 Ω)

As it is shown in figure 15, the new PT design (figure 12) allows achieving ZVS. Although the penalty of achieving ZVS is the lower PT efficiency (from 98% to 94%) and the bigger PT size (from 240 mm^2 to 800 mm^2), no magnetic components are required in the power converter topology.

In addition, high electromechanical coupling coefficient (62%) is obtained.



a. Minimum input voltage (85 Vrms)



b. Maximum input voltage (265 Vrms)

Figure 15. Analysis of zero voltage switching condition considering PT2 design.

Finally, maximum stress value has been obtained in order to accomplish with the PT performance limitation. The maximum stress is obtained for the maximum input voltage. For the considered vibration mode (figure 2), the maximum value is obtained in the middle of the PT thickness. As shown in figure 16, the maximum stress value is 8.5MPa that is lower than the material limit (20MPa).

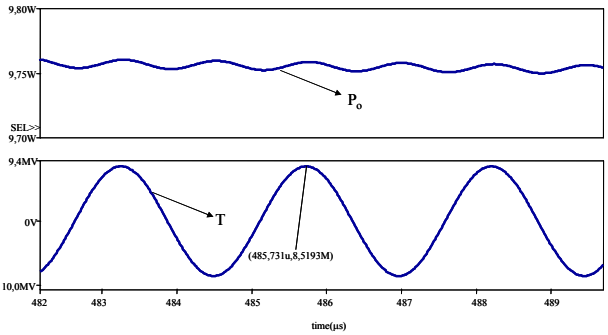


Figure 16. Stress (T) of PT2 design in the middle of PT thickness. V_{IN}=265 V_{rms}

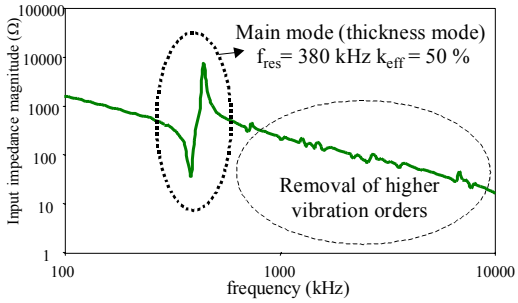
IV. EXPERIMENTAL VALIDATION

A sample of the designed PT has been built to validate the design procedure.

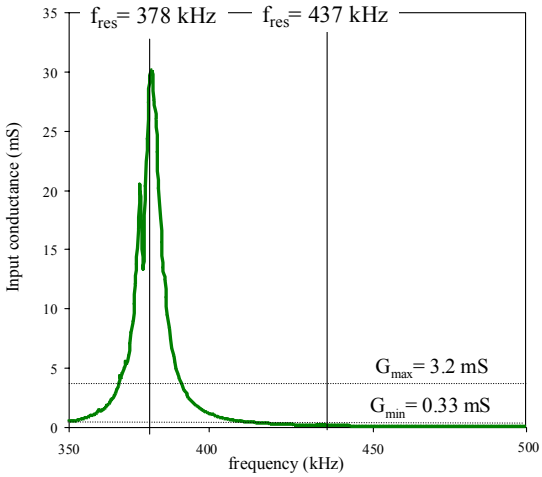
The PT shape (figure 17) is a ring whose diameters have been selected to avoid spurious vibration modes. The external diameter is 25mm and the internal diameter is 19.2mm to obtain the specified area of 200mm^2.

Electrical features of the sample obtained by small signal analysis are shown in figure 18.

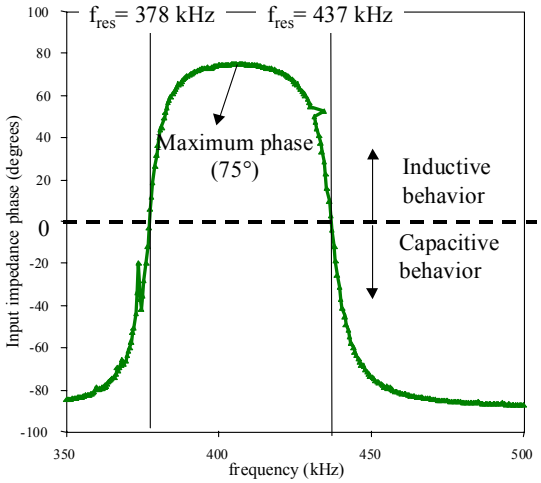
Figure 17. Size of the PT sample.



a. Input impedance magnitude with secondary open



b. Input conductance with its optimum load (14 Ω)



c. Input impedance phase with its optimum load (14 Ω)

Figure 18. Measured sample characteristics

The main mode (thickness mode) has a value of k_{eff} of 50% that is high enough. The lower k_{eff} value compared to simulations with 1D model (62%) is due to the shape influence. Furthermore, higher vibration orders has been removed (figure 18.a) thanks to the proper electrode distribution, as predicted by simulations. The input conductance value (figure 18.b) is achieved (0.33 to 3.2 mS) inside the operating frequency range that is located between resonance (f_{res}) and antiresonance (f_{ares}) frequency. In addition, the expected inductive behavior (maximum phase 75º) is obtained (figure 18.c). Therefore, soft switching transitions (ZVS) without additional magnetic components are obtained as it is shown in figure 19.

However, the penalty of PT design for ZVS is the reduction of its efficiency (93%) and the increment of its size due to the bigger PT area (200 mm^2).

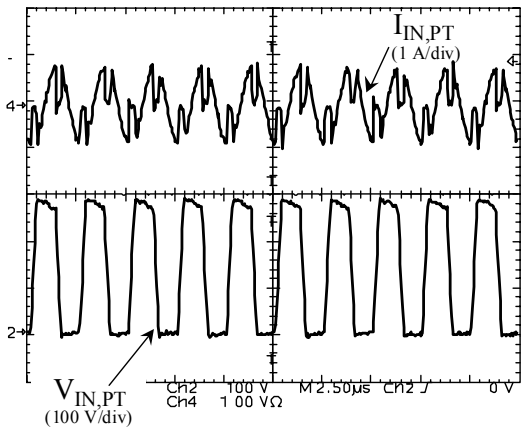


Figure 19. Input voltage ($V_{IN,PT}$) and current ($I_{IN,PT}$) of the PT in the power converter. V_{IN}= 200 V_{ef}. P_o=10 W.

V. CONCLUSION

In this paper, a design procedure for Piezoelectric Transformer (PT) has been proposed and validated.

Topology restrictions determine the electrical requirements of the PT. Once the PT requirements are known, its constructive parameters are defined. These parameters are: the electrode area, the type of material, the number and thickness of the layers and the electrode distribution.

The most important advantage of this PT design procedure is that it is valid not only for sinusoidal driving but also for square driving. Although square driving penalizes PT performance in terms of size and efficiency, improvements in the whole converter are expected (size) since no magnetic components are needed.

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Design Considerations of Multi-Layer Piezoelectric Transformers

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Abstract. **Piezoelectric transformers (PTs) present an attractive solution compared with magnetic transformers because they have alternative characteristics that are appropriate for particular applications, namely high power density and high isolation levels with low EMI content. The behavior of PTs is very dependent on the material type, geometry and number of layers. Since PTs should be used in a power topology, it is necessary to establish design rules in order to select the proper specifications of the PT for each particular application. This work presents some design guidelines as well as the description of the influence of several constructive parameters on the behavior of the multi-layer PTs.**

I. INTRODUCTION

Piezoelectric transformers present several characteristics that make them attractive for particular applications. However, they are not widely applied in many electronic circuits. So far, they are only commercially used in some particular applications with high voltages and high isolation levels (flat screens for computers). The power limit depends on the size of the PT, but in practical cases it is limited to a few watts. Although PTs have not been commercially applied in DC/DC or AC/DC converters, there are publications about this topic [1].

The first step in any PT design is the identification of the application. In this work, the PT is applied to build a power converter designed to load the batteries of mobile phones. The power range of this application is 12 W and input voltage between 100 V_{DC} and 200 V_{DC}. However, the design rules extracted from this particular case can be extended to other applications. The main advantages of the use of a PT in this particular application are: very high power density, small size and weight and low EMI. Since the AC adapters for mobile phones should be as light and small as possible, PTs are a nice proposal to achieve these goals.

The figure 1 shows the PT situation in the power converter. Although there is DC voltage in the input and output of the converter, it is possible to "adapt" the voltage in the input of the PT using an "Impedance Matching" networks. Therefore, it will be assumed that sinusoidal waveform is applied to the PT and an equivalent resistance is connected at the output, as it is shown in figure 1.

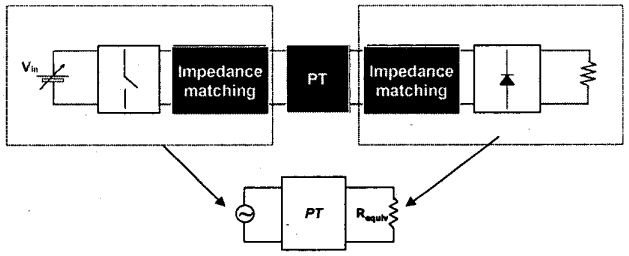

Figure 1. Equivalent system to be analyzed

Therefore, the design procedure should start with the electrical specifications of the power converter where the PT is used. In the next section, it will be shown that the main design goals are the efficiency, electromagnetic coupling, input impedance, physical limitations and temperature rise (power dissipation). The design procedure should be focused in the achievement of all these specifications using degrees of freedom like area, length, number of electrodes (layers), etc.

The PT structure selected for this application is shown in figure 2. Figure 3 presents a photo of the final prototype. The main characteristics of this structure are as follows:

- One layer of primary at one side of the insulator layer with the electrodes at the edges of this primary layer.
- Insulator layer between primary and secondary.
- Multi-layer secondary at the other side of the insulator layer.
- Bulk (not polarized material) layer to obtain the proper PT length.
- The PT is vibrating in thickness mode.

It is not the goal of this paper to evaluate the advantages and drawbacks of this particular structure. The main objective of this work is to obtain design rules to be applied in multi-layer PT designs.

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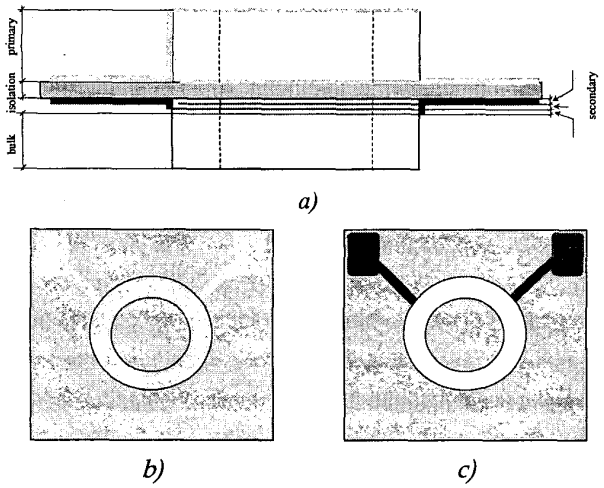

Figure 2. Structure of the multi-layer PT.
a) Lateral view. b) Top view (primary side, one layer). c) Bottom view (secondary side, multi-layer).

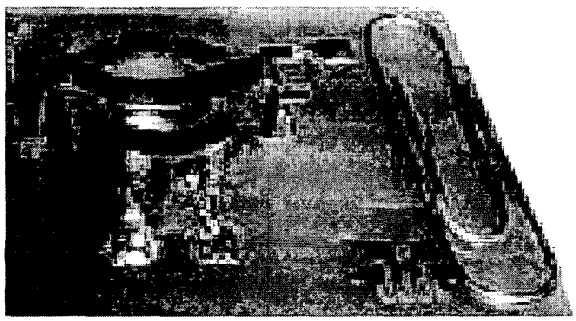

Figure 3. Photograph of the PT.

II. GENERAL PROCEDURE TO DESIGN PTs

Once the selected application is defined, the next step is to establish a design procedure in order to develop the PT. The main steps of this procedure are presented below.

A. Design goals:

The first step is to identify the specifications of the PT in order to work in the power converter. There are three main parameters that are required in order to design a valid PT for each application:

***Adapting the PT design to output conditions*: Calculation of the equivalent load to be connected to the output of the PT.** The influence of the load in the behavior of the PT is enormous. Therefore, it is necessary to know the equivalent load connected to the PT output before the design, because this design is determined by the load. The PT should be designed in order to present maximum efficiency with the connected load. The load needed to obtain maximum efficiency in each particular PT is known as **"optimum load".** It is convenient to design for the maximum load specifications, mainly because of the thermal limit.

***Adapting the PT design to input conditions:* Calculation of the input conductance.** Since the power that should be transferred by the PT for a given input voltage is a specification, the PT parameter that limits the power that can be transferred is the real part of the input admittance (input conductance). Therefore, for a given input voltage, it is possible to determine what should be the input conductance of the PT in order to handle the proper power (equation 1).

$$P_{in} = V^2_{in} * \text{Input Conductance} = P_{out}/\text{efficiency} \qquad (1)$$

Selection of the operating frequency. This frequency should be selecting accounting for the total losses in the converter (switching losses) as well as the size of the PT.

Figure 4 shows the behavior of a PT vs frequency for different loads. It can be seen that depending on the load, the behavior of the PT is different. By definition of optimum load, if the optimum load is connected to the PT, the efficiency is higher. The input impedance curve is flatter connecting the optimum load. It can be also seen that the input conductance is lower using the optimum load.

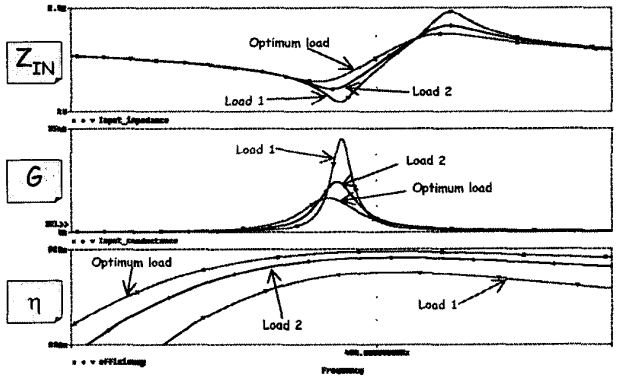

Figure 4. Input impedance (Z_{in}), input conductance (G) and PT efficiency (η) vs frequency for three different loads.

B. Degrees of freedom.

The design goals mentioned above can be obtained using the following degrees of freedom:

Material. Depending on the power density and suppression of spurious modes, there are two main materials to be used: Lead-Titanate and PZT. First one presents less spurious modes but lower power density. In this work, PZT material has been selected

Length. The length of the transformer is mainly related with the desired resonance frequency. Once the resonance frequency is selected, the total length can be determined.

Area. The area of the transformer is mainly related with the power level to be transmitted. The value of the input impedance also depends strongly on the area. The higher the power to be transmitted, the larger the transformer.

Shape. The shape should be selected in order to eliminate the spurious modes near to the operating (resonance) frequency. Lead-Titanate material is not isotropic, and "block" shapes are usually enough to remove spurious modes. However, if PZT material is used, it is needed to select the proper shape (making a hole) in order to reduce vibrations in the "horizontal" and "radial" directions.

Number of layers. Using one layer in primary, the selection of the number of layers for secondary is mainly determined by the optimum load for the transformer operation (load with maximum efficiency), that should be as close as possible as the equivalent load connected to the secondary. However, the number of layer affects the value of the input and output impedances of the component. Multi-layer transformers are specially recommended when a high voltage ratio is needed between input and output.

Electrodes separation and isolation layer thickness. As it will be shown in the section III, these values are very important in order to determine the input and output impedances, gain and efficiency of the transformer. The input impedance is very affected by the position and separation of the primary electrodes. Bulk zones (non-polarized material) can be added in order to keep constant the total length modifying the position and thickness of the layers.

C. Parameters to be controlled.

It is needed to use a model in order to simulate the behavior of the PT and to establish an iterative procedure in order to adjust different key parameters. The main parameters to be adjusted during the design procedure are commented below.

1. The transformer should be design in order to obtain an **optimum load** as close as possible as the equivalent load connected to the transformer in our application.
2. The **real part of the input admittance (input conductance)** should be higher than the one needed to transfer the proper power. If input conductance is smaller than the specified value, the transformer will not be able to transfer the required power. This value is directly related with the voltage gain, which should be higher than a particular value in order to obtain the proper voltage and power at the output of the transformer.

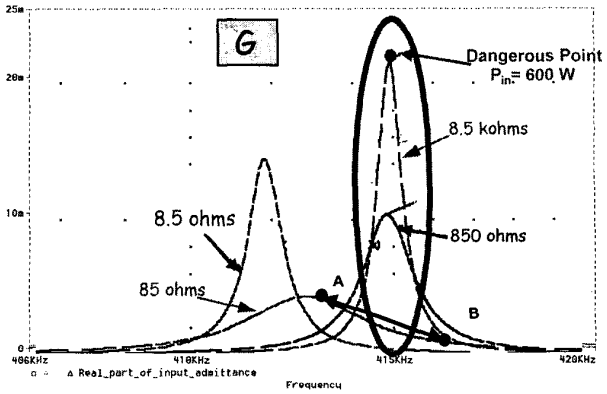

Figure 5. Input conductance vs frequency for several loads.

Figure 5 shows the input conductance vs frequency for different loads connected to the PT. It is assumed that the control scheme was working between points A and B in order to regulate the load voltage. It should be noticed that if the load changes from the optimum one (85 Ω in this particular case) to another one (for example 8.5 kΩ), the control curve now describes a different law. This means that "dangerous" points from the point of view of the input conductance should be avoided in order to protect the PT. If the input conductance is very high, the power introduced in the PT could be enormous and the heat dissipation could not be enough.

3. The **efficiency** and the **electro-mechanical coupling (K_{eff})** should be as high as possible. The K_{eff} value determines the amount of electrical energy that is converted into mechanical energy in a block of piezoelectric material. Increasing this parameter, the use of the energy is more efficient, minimizing circulating currents. Typical values of this parameter are around 30%-45% in practical designs.

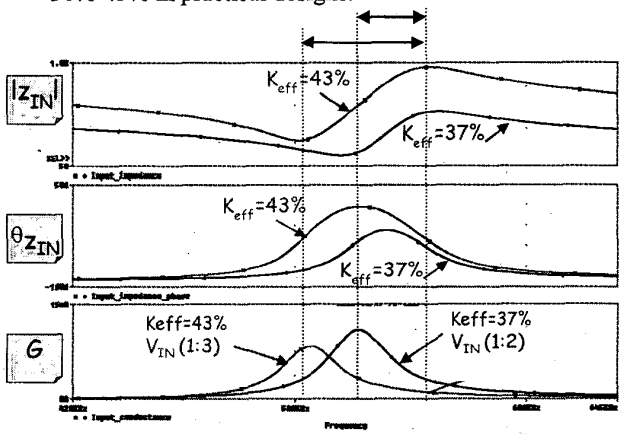

Figure 6. Module ($|Z_{in}|$) and phase (θ_{Zin}) of the input impedance and input conductance (G) vs frequency for two PTs with different effective coupling coefficients.

Figure 6 shows the behavior of the PT vs frequency for different values of the effective coupling (K_{eff}). Different conclusions can be extracted from this figure:

- The separation of the resonance and anti-resonance frequencies is higher for higher K_{eff} value. The working frequency range (between resonance and anti-resonance frequencies) is wider for higher K_{eff} values.
- The phase is higher (closer to 90°) for higher K_{eff} values. This means that the ZVS implementation is more feasible for higher K_{eff} values.
- In the working frequency range (between resonance and anti-resonance frequencies), the variation of the input conductance is higher for higher K_{eff} values. Therefore the input voltage variation can be higher if K_{eff} is higher.

4. The adequate behavior in large signal is mainly determined by the physical limitations of the component. These limitations are: maximum **stress**, maximum **strain**, maximum **electric field** and maximum **electric displacement**. The position of the electrodes should be determined in order to accomplish with all these limitations.
5. **Minimum displacement at the isolation layer**. The transformer is going to be mounted on a PCB fixing it at the isolation layer. The performance of the transformer worsens if the vibration of the PT is limited. Therefore, a design goal is to have small displacement at the isolation layer. This can be achieved selecting the proper vibration mode and placing the isolation layer in the adequate situation.
6. Another important point that should be accounted is the **temperature rise** in the component. The thermal dissipation should be high enough to avoid a high temperature rise in the component. Since the behavior of PTs is strongly affected by the temperature, this point is extremely important in any PT design. The best way to limit the temperature rise is to limit the power losses by limiting the minimum efficiency. Figure 7 shows the efficiency of the PT vs frequency for different temperatures. It can be seen that in the flatter part of the curve (higher efficiency) the higher the temperature the lower the efficiency.

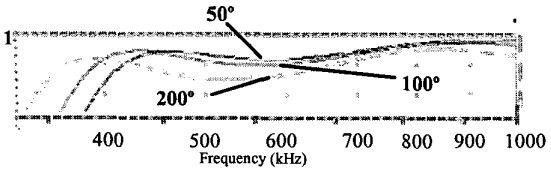

Figure 7. Efficiency vs frequency at 25, 100 and 200°C.

III. SENSITIVITY ANALYSIS

The variation of the constructive parameters has a great influence on the behavior of the component. Unfortunately, all parameters should be considered simultaneously, and the variation of any geometrical parameter affects to several electrical parameters. The purpose of this section is to summarize the main effects of several constructive parameters on the component behavior. A 1D model based on transmission lines has been used in order to carry out this sensitivity analysis. This model accounts for all the effects in the vibration direction (thickness mode). Therefore, spurious modes are neglected.

In all these analyses, the maximum theoretical power presented in the tables is always above the real maximum power of the component because there are physical considerations (electric field, temperature rise, etc) that are the ones that limit the maximum power. Therefore, this value represents the maximum theoretical power that the component is able to transmit from the point of view of the input conductance.

A. Variation of the Area

In this analysis the area perpendicular to the thickness of the PT is modified, keeping constant the rest of the physical and geometric parameters of the PT. Results of this analysis are presented in table I.

Table I

Area (mm^2)	*Req_op* (ohm)	*Efficiency* (%)	*Keff* (%)	*Pmax* (W)
20	247.321	97.904	38.8	105.303
25	197.859	97.904	38.8	131.622
30	164.875	97.904	39.1	158
35	141.332	97.904	33.6	184.406
40	123.629	97.904	41.0	206.72
45	109.914	97.904	39.1	236.984
50	98.907	97.904	39.1	263.094

The results of table I allow obtaining the following conclusions:

- The bigger the area, the lower the optimum equivalent resistance.
- Efficiency (near the resonance frequency) keeps almost constant when the area changes.
- The bigger the area, the higher the maximum power that is able to handle.

B. Number of layers in secondary side

This analysis consists on the modification of the number of electrodes in the secondary side (number of layers). The

thickness of the layers is 0.3 mm. In order to keep constant the length of the whole PT, the thickness of the secondary bulk zone has been modified accordingly to the number of secondary layers.

Table II

Number of layers	Req_op (ohm)	Efficiency (%)	Keff (%)	Pmax (W)
1	386.872	94.595	30.4	215.626
2	205.204	97.141	35.9	127.479
3	143.932	97.904	39.1	180
4	108.675	98.16	34.2	206.775
5	86.369	98.145	33.6	203.731
6	71.738	97.907	32.3	176.773

The results of this analysis are presented in table II. The next conclusions can be extracted:

- The higher the number of layers, the smaller the optimum equivalent resistance.
- The efficiency and K_{eff} present a maximum value.

C. Distance between the electrodes in secondary side

A PT with three layers has been considered for this study. In this analysis, the thickness of the three secondary layers is modified, with the restriction that all the layers have the same thickness, keeping constant the total length of the PT (modifying the secondary bulk zone thickness. Results of this analysis are presented in table III.

Table III

Layer Thickness (mm)	Req_op (ohm)	Efficiency (%)	Keff (%)	Pmax (W)
0.1	42.94	94.595	30.4	63.038
0.2	91.351	97.142	35.9	127.563
0.3	143.932	97.904	39.1	180.837
0.4	194.064	98.155	40.3	207.558
0.5	242.863	98.139	39.9	207.76
0.6	286.436	97.904	38.3	178.461

From the results presented in table III, the next conclusions can be extracted:

- The larger the thickness of the secondary layers, the higher the optimum equivalent resistance
- Efficiency, K_{eff} and maximum output power present a maximum value.

D. Insulator thickness

In this analysis the insulator thickness will be modified. The length of the whole device has been kept constant varying the secondary bulk zone thickness. The insulator thickness has been varied in a range that allows appropriate performance of the device. Results of this analysis are presented in table IV.

Table IV

Insulator Thickness (mm)	Req_op (ohm)	Efficiency (%)	Keff (%)	Pmax (W)
0.1	135.384	98.373	41.3	193.199
0.2	138.462	98.358	41.0	197.188
0.3	142.894	98.318	40.8	203.935
0.4	144.083	98.261	40.8	203.935
0.5	143.073	98.196	40.3	194.454
0.6	143.618	98.068	39.3	187.718
0.7	143.932	97.904	39.1	180.837

The following conclusions can be extracted:

- Efficiency and K_{eff} slightly decrease if insulator thickness is increased.
- The larger the thickness of the insulator thickness, the higher the optimum equivalent resistance
- The theoretical power to be transferred to secondary presents a maximum value.

E. Distance between the electrodes in primary side

In this analysis the distance between the electrodes in the primary side has been modified from 0.1 to 1.2 mm, keeping constant the total length of the PT by making thinner the secondary bulk zone. Results of this analysis are presented in table V.

Table V

Dist between Electrodes (mm)	Req_op (ohm)	Efficiency (%)	Keff (%)	Pmax (W)
0.1	3.566	54.7	5.1	7.701
0.2	31.875	72.2	5.8	54.568
0.3	82.596	81.81	6.0	133.473
0.4	112.669	90.07	7.0	209.752
0.5	134.104	93.83	8.4	209.752
0.6	127.869	95.59	8.4	198.708
0.7	135.649	96.56	10.9	199.507
0.8	135.649	97.06	12.9	199.507
0.9	143.686	97.54	14.6	199.507
1	140.648	97.63	17.5	199.507
1.1	145.734	97.66	20.0	196.037
1.2	143.932	97.704	22.6	180.837

This analysis allows concluding that:

- The higher the distance between the primary electrodes, the higher the optimum equivalent resistance, the efficiency and the K_{eff} value.
- The maximum output power presents a maximum value.

F. Thickness of secondary bulk zone.

In this analysis, the thickness of the secondary bulk zone is varied from 0 to 1 mm. To keep constant the total length of the PT, the distance between electrodes in the primary is reduced gradually. Results of this analysis are presented in table VI.

Table VI

Thickness Secondary Bulk (mm)	*Req_op (ohm)*	*Efficiency (%)*	*Keff (%)*	*Pmax (W)*
0	143.507	85.076	44.9	22.399
0.1	140.052	89.544	43.3	33.504
0.2	139.99	92.275	41.9	46.613
0.3	140.784	94.055	41.0	62.838
0.4	139.363	95.344	39.6	81.085
0.5	138.569	96.247	38.8	100.472
0.6	142.422	96.826	38.6	126.411
0.7	142.308	97.311	38.6	150.691
0.8	141.059	97.668	38.9	164.506
0.9	143.932	97.904	39.1	180.837
1	145.734	98.072	38.9	196.307
1.1	140.648	98.235	38.6	199.507

The next conclusions can be extracted:

- The optimum equivalent resistance does not vary significantly.
- Efficiency grows considerably when the thickness of the secondary bulk zone increases.
- K_{eff} decreases slightly as the thickness of the secondary bulk zone increases.
- The maximum output power increases when the thickness of the secondary bulk zone increases.

IV. CONCLUSIONS

This work presents several design guidelines to design multi-layer piezoelectric transformers. A design procedure is proposed in order to design a PT for given electrical specifications.

The following *steps* have been proposed:

1. Selection of the proper PT **input impedance** in order to adapt it to the input conditions: input voltage and power.
2. Calculation of the **equivalent load** connected to the PT in order to optimize the PT efficiency for that load.
3. Selection of the **operating frequency** accounting for both, the PT and converter losses

The *degrees of freedom* available to design the PT are mainly:

- **Material, length, area, shape, number of layers** and **separation among layers.**

The *parameters* that should be controlled during the design procedure are the following ones:

- **Optimum load, efficiency, input impedance, electromechanical coupling coefficient, physical limitations** and **temperature rise.**

A sensitivity analysis where several constructive parameters have been modified has been also presented. This analysis allows us to extract some conclusions about the influence of each parameter on the PT behavior. The design of the PT is very complex because its behavior depends on many parameters simultaneously. Therefore, conclusions drawn from this analysis are applicable to design multi-layer Piezoelectric Transformers.

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Interleaving of electrodes in Piezoelectric Transformers

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***Abstract*- Piezoelectric transformers (PT) have become interesting for miniaturizing low power AC/DC or DC/DC converters. In this paper, interleaving of primary and secondary electrodes of the PT is analyzed in order to optimize the converter solutions based on PT. One of the problems to achieve a competitive PT converter is the additional magnetic components necessary to drive properly the PT. The main advantage of interleaving structures comparing to conventional one is that it allows to reduce or even to eliminate these additional elements, which is a step forward to improve converters based on PT.**

I. INTRODUCTION

Piezoelectric Transformers (PT) are becoming an alternative to magnetic transformers in some particular applications where size and weight of the power converter are critical issues. The main features of these devices are high power density, high isolation levels and low EMI content. These characteristics make PTs very attractive for low power DC/DC or AC/DC converters [1-3].

The use of additional magnetic components becomes necessary in most applications to properly drive the PT. This fact reduces the advantages of using this technology. However, applying interleaving to the PT electrodes can reduce the energy handled by the magnetics.

The interleaving approach is based on the optimization of the position of the primary and secondary electrodes. In this paper, the advantages of using the interleaving approach comparing with the conventional PT structures are analyzed. It is important to highlight that the goal is to reduce the size of the converter.

II. GENERAL ISSUES OF POWER TOPOLOGY

In order to develop a competitive converter, the topology considered for this analysis is the one shown in Figure 1. It is a Half Bridge stage, which is a topology widely used in PT applications.

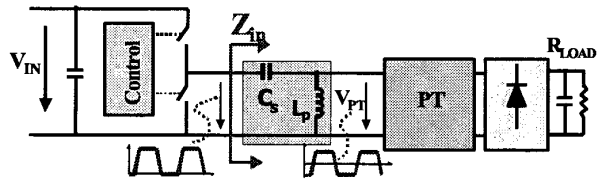


Figure 1. Power topology with an input matching network.

The operating frequency range of the PT is located between resonance (f_{res}) and antiresonance (f_{ares}) frequency of the considered vibration mode.

In Figure 2, the magnitude and the phase of the PT input impedance in the mentioned frequency range is shown.

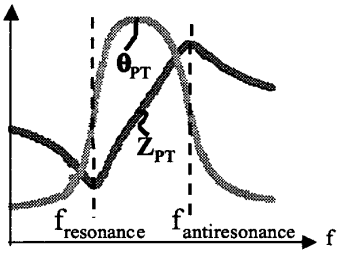


Figure 2. Magnitude (Z_{PT}) and phase (θ_{PT}) of the input impedance of the PT versus frequency. Operating frequency range.

The PT fixes the switching frequency of the HB within its operating frequency range. Since PT is driven with squared voltage, Zero Voltage Switching (ZVS) condition becomes critical in order to avoid high current peaks at the input of the PT. These current peaks worsen PT performance since the PT losses increase too much. Therefore, an input matching network, consisting on a series capacitor and a parallel inductor, is added between the HB and the PT to provide soft voltage transitions [4].

In addition, ZVS is suitable to diminish turn-on losses in the switches and to increase the converter efficiency. These losses are important because of the high switching frequency.

The phase of the input impedance (Zin) seen by the HB should be positive to allow achieving ZVS. Therefore, an inductive behavior at the output of HB is required. Nevertheless, if PT is designed to provide this inductive behavior, the input matching network can be avoided and magnetic-less converter (Figure 3) can be obtained [4].

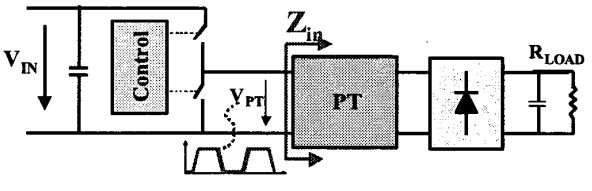


Figure 3. Magnetic-less converter topology.

PT is driven with squared voltage that contains harmonics of several orders. If the spurious modes are

excited by input voltage harmonics, PT performance worsens because it vibrates in different directions.

Another important PT feature to design properly the converter is its input conductance (G_{PT}) that is the real part of the input admittance. Given a PT-handled power (P), the input voltage (V_{IN}) that can be applied to the PT is related to the input conductance (G_{PT}) according to the following expression:

$$P = G_{PT} \times V_{IN}^2 \quad (1)$$

The converter control law can be drawn out from the PT input conductance (Figure 4): an increment in the input voltage of the converter involves an increment in the switching frequency of the converter in order to keep constant the power supplied to the load.

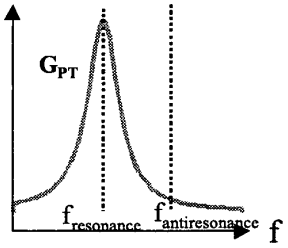


Figure 4. Input conductance of PT versus frequency.

III. New PT Physical Structure

As seen in previous paragraph, the electrical features of PT are very important to design properly the power converter. A new PT geometry is analyzed to adapt the device to the requirements of the topology even though the performance of PT is penalized.

On one hand, symmetrical structures related to displacement distribution allow to avoid spurious modes. On the other hand, bigger power density can be obtained by placing the electrodes in the point of maximum stress ([5]).

Both characteristics can be obtained by employing interleaving concept

A. Description of interleaving concept

PTs are based on the fact that the piezoelectric phenomenon is a direct and inverse effect. Therefore, a primary part (actuator) converts the input electrical energy into mechanical energy and the secondary part (sensor) transforms this energy into electrical one. The conventional structure joins sensor and actuator in a single device as shown in Figure 5.

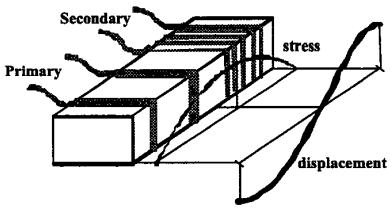


Figure 5. Conventional structure.

The technique of interleaving is based on the physical position of the electrodes of primary and secondary. Interleaving is obtained when the electrodes of one part of the transformer are placed among the electrodes of the other part. In this paper, characteristics of interleaving concept have been analyzed in first order of thickness extensional vibration mode. This concept has been applied to other vibration modes ([6],[7]).

The analytical study of these devices is very complex due to the influence of the constructive parameters. Finite Element Analysis tools combined with electrical models are required to analyze its behavior and help to improve the PT features by sensitivity analysis of the number of electrodes, electrode position, etc ([8]). The distribution of the PT stress and displacement for the considered vibration mode are shown in Figure 5. For this particular case, there are two possibilities to make the structure symmetric respect to the displacement and also put the electrodes in maximum stress point:

1. Type I interleaving (Figure 6): the mechanical energy generation is improved by placing primary in the middle point where the stress and vibration velocity are maximum.

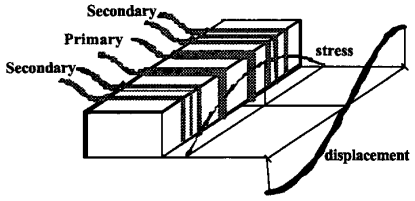


Figure 6. Type I interleaving structure.

2. Type II interleaving (Figure 7): secondary could be placed at the same point aforementioned in order to improve the reception of the mechanical energy.

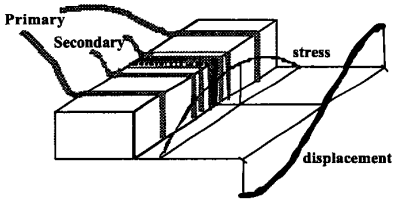


Figure 7. Type II. Interleaving structure.

This improvement in the management of the energy by the device can be evaluated with the electromechanical coupling coefficient (k_{eff}). This parameter accounts for the relation between converted energy by piezoelectric effect and the total energy that has been introduced in the device [9]. Furthermore, interleaving of the electrodes makes possible to position the PT structure symmetrically related to the displacement distribution. This symmetry can be used to reduce the spurious vibration modes.

All these aspects are explained by applying the concept on a simple structure that consists on a single layer of primary and secondary.

In Figure 8, the different orders of the main vibration mode for conventional structure have been represented. It is shown that k_{eff} can be increased from 35 % to 40% by improving the position of one side of the transformer related to the stress and displacement characteristic.

Nevertheless, none of the orders of main vibration mode is avoided. However, interleaving technique allows increasing k_{eff} value between 40% and 50% depending of the interleaving type as shown in Figure 9. In addition to this, both types of interleaving eliminate second order of the main vibration mode due to the symmetry. Additional vibration modes can be considered as spurious modes since they can worsen the PT performance.

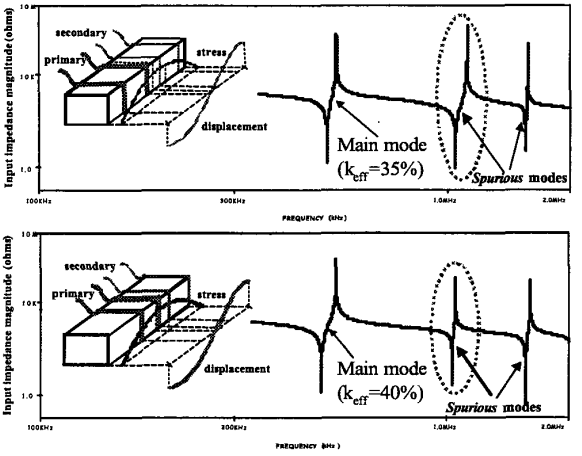


Figure 8. Input impedance magnitude. Influence of the symmetry in conventional structure on the spurious modes and k_{eff}.

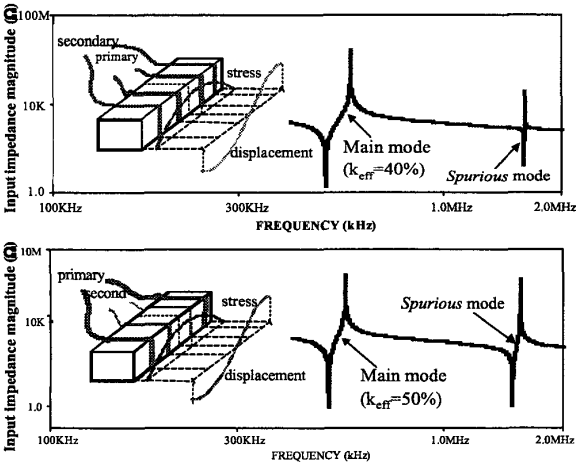


Figure 9. Input impedance magnitude. Influence of interleaving on the spurious modes and k_{eff}.

B. Advantages of interleaving

Interleaving concept improves some electrical features comparing to the conventional PT structure.

The applications that have been considered require a step-down voltage ratio in the PT. Therefore, several layers in the secondary side of the PT are required. In order to analyze the advantages of this technique, three different PT designs based on the different approaches have been compared by simulations with models: conventional structure (Figure 5), Type I interleaving (Figure 6) and Type II interleaving (Figure 7).

The main advantages of the new approach are explained in this section.

1. Reduction of the spurious modes.

The symmetry in the position of the primary and secondary electrodes related to the displacement distribution allows eliminating spurious vibration modes as it has been explained in previous paragraph. Therefore, conventional structure presents more spurious modes than interleaving structures as seen in Figure 10.

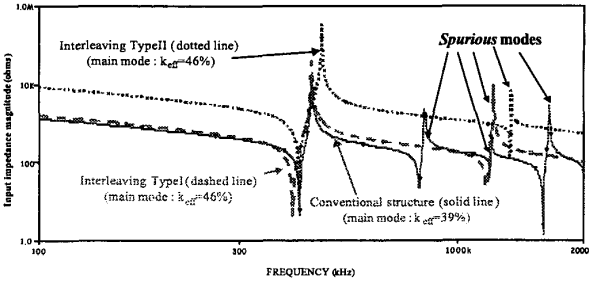


Figure 10. Input impedance magnitude for conventional and interleaving structure. Comparison of the spurious modes and k_{eff}.

2. Higher electromechanical coupling coefficient

As said before, the optimization in the position of the electrodes improves the conversion of the energy. Therefore, the value of k_{eff} is higher with interleaving (46%) than with conventional structure (39%) as it is shown in Figure 10.

3. "Good" inductive behavior

As mentioned above, an inductive behavior of the PT improves the whole converter, since it allows switches to achieve ZVS condition.

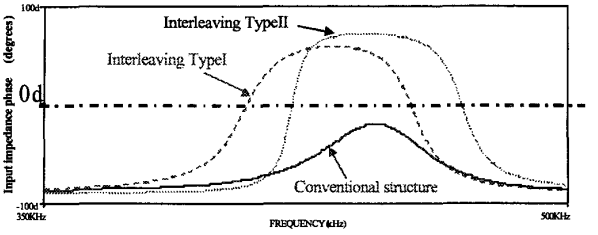


Figure 11. Input impedance phase for conventional and interleaving structures. Comparison of the inductive behavior.

An inductive behavior implies that the PT has an impedance phase over zero degrees within the operating frequency range. As seen in Figure 11, the input impedance phase of the PT is over zero degrees with interleaving approaches, but it is under zero degrees with conventional structure. Therefore, interleaving technique improves the inductive behavior of the PT.

The drawback is the penalty in the PT efficiency due to the increment of the circulating energy.

4. Input conductance

The input conductance of the different designs is shown in Figure 12. As said above, the input conductance of the PT and the input voltage of the converter are related by equation (1).

Larger distances between primary electrodes provide low G value. Hence, interleaving structure of type I is more

appropriate for low input voltage application while type II structure is suitable for high input voltage applications.

In addition, the variation of the input conductance within the operating frequency range determines the input voltage range achievable by the converter. Since the slope of input conductance is stronger with interleaving approach than with conventional structure, the input voltage variation is bigger with interleaving. The input voltage range with conventional structure is 1:2, while Type I interleaving allows 1:3 voltage ratio and Type II interleaving allows 1:3.6 voltage variation within the operating frequency range.

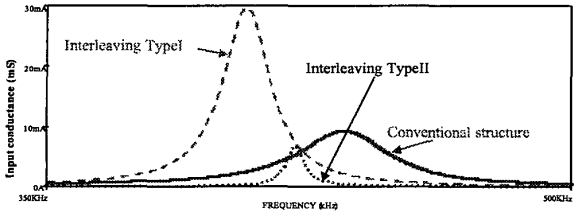
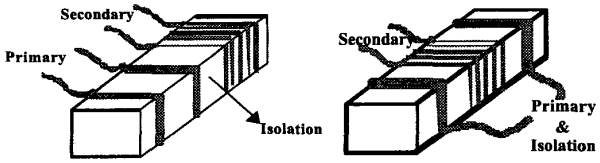


Figure 12. Input conductance for conventional and interleaving structures.

The **Type II** interleaving structure has two additional advantages:

1. Suppression of the isolation layer

Conventional structures require the inclusion of an inactive layer in order to provide electrical isolation between primary and secondary side. Due to multilayer in secondary side, Type I requires the isolation layer as well. However, as it can be seen in Figure 13, interleaving structure of Type II does not need to introduce another piezoelectric layer to separate primary and secondary. The relative position of primary and secondary electrodes allows primary to behave also as an isolation layer. The suppression of this layer improves the performance of the PT.



Conventional structure Interleaving structure.Type II

Figure 13. Electrical isolation

2. Higher breakdown voltage

Piezoelectric material between two electrodes behaves as a capacitor. The bigger the separation between the primary electrodes, the higher the input breakdown voltage. Considering the same PT length, the separation among the primary electrodes is larger with Type II interleaving approach than with conventional structure.

IV. Experimental Results

In order to verify the electrical advantages of interleaving that have been previously described, samples with conventional structure and with interleaving structure have been built.

A. Description of the samples

The samples are ring-shaped blocks (Figure 14) with similar transversal area (around 60 mm^2) and thickness (around 3.9 mm).

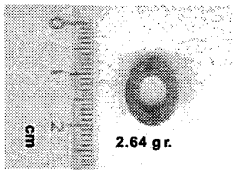


Figure 14. Sample dimensions.

Sample A belongs to conventional structure group (Figure 5). It has four electrodes in primary and fourteen electrodes in secondary side. Sample B has been built with an interleaving structure of type I (Figure 6). It has the same primary side as sample A and the secondary side contains twelve electrodes splitted in two groups of six electrodes at both sides of primary.

The resistive load that involves the maximum efficiency in the PT is named optimum load (R_{opt}). The R_{opt} of both samples is very similar. R_{opt} of Sample A is 7.5 ohms and R_{opt} of Sample B is 5 ohms.

B. Validation

The input impedance magnitude of both samples under no load conditions is shown in Figure 15. It can be seen that, **sample with interleaving** (Sample B) **has lower number of spurious modes**.

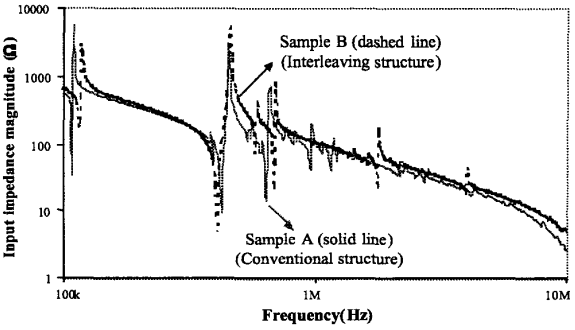
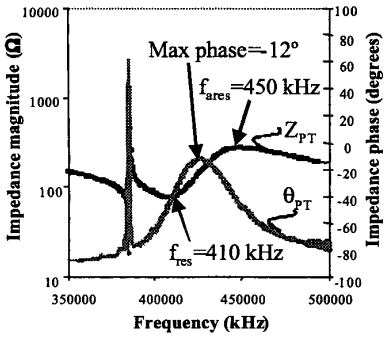
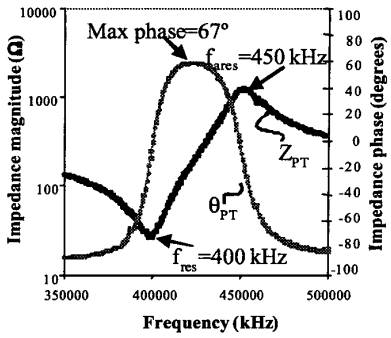


Figure 15. Frequency response of the input impedance of both samples at no load condition

The small signal test of the samples with the optimum load is shown in Figure 16. As seen, **the value of k_{eff} of sample with interleaving structure is bigger** (46%) than the one with conventional structure (42%). In addition to this, it is shown that the input impedance phase is much higher with interleaving approach. Sample B has a maximum input impedance phase of 67° (inductive behavior) while maximum input impedance phase of sample A is −12° (capacitive behavior). Furthermore, there is a *spike* in the input impedance magnitude of Sample A very close to the main resonance frequency that is due to a spurious mode.



Sample A. Conventional structure



Sample B Interleaving structure (Type I)

Figure 16. Magnitude (Z_{PT}) and phase (θ_{PT}) of the input impedance measured with the optimum resistive load.

Figure 17 shows the input conductance value of both samples. Taking into account equation (1), it can be concluded that Sample B, with **interleaving structure, can be applied for** a lower input voltage values and **higher input voltage variation** than Sample A, with conventional approach.

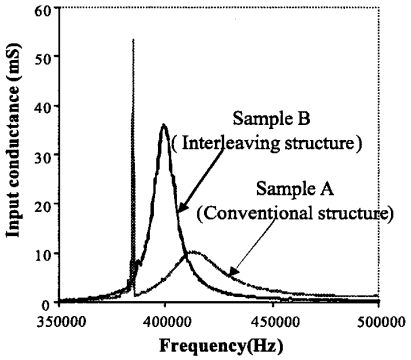


Figure 17. Input conductance with optimum load.

Several power tests have been done in order to validate the different behavior characteristics of interleaving compared with conventional structures in terms of the performance inside the topology. Sinusoidal driving test (Figure 18) has been done in order to analyze the differences in the values and the plot of the efficiency.

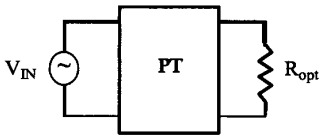


Figure 18. Power test: Sinusoidal driving conditions.

The PT efficiency and the input voltage variation of the samples have been measured with the same output load of 5 watts. As seen in Figure 19, the efficiency of Sample B is lower, since the improvement of the inductive behavior implies a higher circulating energy that penalizes the PT efficiency. Nevertheless, the PT efficiency of interleaving structure (sample B) is flat and high enough comparing to conventional structure (Sample A) inside the operating frequency range.

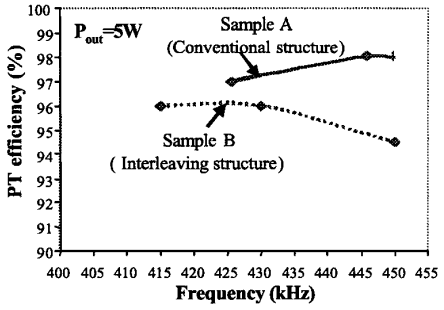


Figure 19. Comparison of measured efficiency. Sinusoidal driving test.

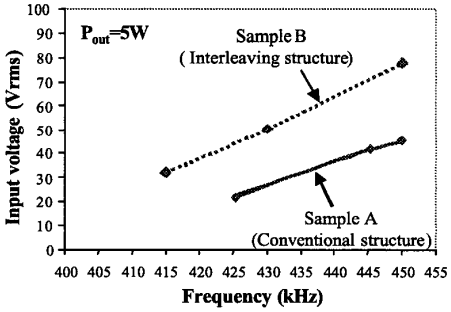


Figure 20. Comparison of measured input voltage variation. Sinusoidal driving test.

On the other hand, the input voltage variation is bigger with Sample B (interleaving structure) than with Sample A (conventional structure) as mentioned before. In Figure 20, it can be seen that Sample A allows 1:2 input voltage ratio while Sample B allows a variation of 1:2.5. These values are very close to the ones predicted by models in previous section.

The cost of the transformer with interleaving is lower since similar optimum resistive load is achieved with a lower number of electrodes.

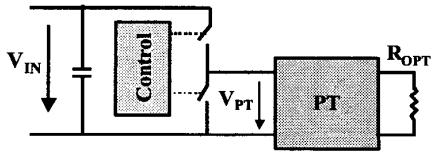
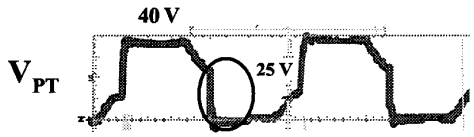


Figure 21. Square driving test. Magnetic-less topology.

In order to compare the PT capability to provide ZVS, square-driving test with magnetic-less topology (Figure 21) has been carried out.

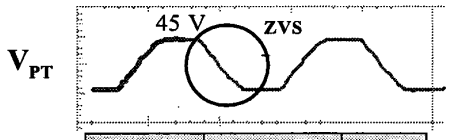
As seen in Figure 22, PT efficiency is reduced more than 10 points (from 97% to 84 %) when the turn-on voltage at the input of the PT is 25 V. Therefore, the hard switching in PT input voltage reduces significantly the efficiency of the device. An additional parallel inductor with similar size of the PT is necessary to avoid hard voltage transitions and to drive properly the PT.



$V_{in,DC}$(V)	$P_{OUT,PT}$(W)	η_{PT}(%)
40	1.8	84

Figure 22. Magnetic-less with Sample A and R_{LOAD}=7.5 ohms Hard-switching with conventional structure.

As it can be seen in Figure 23, the sample with interleaving (Sample B) allows ZVS condition in the switches of the half bridge stage. Therefore, **the interleaving structure provides "good" inductive behavior to the PT**. However, square driving reduces around 3 points PT efficiency comparing with sinusoidal driving (from 96 % to 93%). If the PT is designed to achieve ZVS condition, the additional magnetic component at the input of the PT can be avoided.



$V_{in,DC}$(V)	$P_{OUT,PT}$(W)	η_{PT}(%)
45	2	93

Figure 23. Magnetic-less with Sample B and R_{LOAD}=5 ohms. Soft-switching with interleaving structure.

As mentioned before, conventional structure (Sample A) requires an additional matching network to provide ZVS at the input of the PT. In order to estimate the influence of this matching network on the converter size, two converters based on Sample A and Sample B are designed for the same input voltage variation (1:2) and the same output power (3W). The first one requires the input matching network (Figure 1), since it is based on a conventional PT structure (Sample A). The second one, based on interleaving structure (Sample B), does not need the input matching network (magnetic-less, Figure 3). Magnetic-less converter involves a reduction of the converter volume around 40%. This size reduction is due to the converter height decrement (from 5.8 mm to 4 mm) achieved by the elimination of the parallel inductor (E6.3/2.9/2 core). In addition, a converter area reduction of 9% (from 300 mm^2 to 272 mm^2) is achieved with magnetic-less topology.

Therefore, magnetic-less approach takes benefit of the PT features.

V. Conclusions

In this paper, interleaving of the electrodes of primary and secondary side in thickness extensional mode has been proposed and validated. The main advantages of this approach comparing with the conventional structure are:

- Reduction of the spurious modes
- Bigger electromechanical coupling coefficient (k_{eff})
- "Good" inductive behavior for achieving Zero Voltage Switching condition.
- Higher breakdown voltages are achieved by applying Type II interleaving structure.

The electrical characteristics of interleaving PT structures allow to minimize or even eliminate the magnetic of the input-matching network that is required for square driving of the PT. The converter size is reduced by eliminating the input matching network. Therefore, interleaving technique can improve the goodness of PT-based solutions for some applications.

Acknowledgements

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Experimental Validation of an Optimized Piezoelectric Transformer Design with Interleaving of Electrodes

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***Abstract*— Interleaving of electrodes in Piezoelectric Transformers (PTs) consists on placing the electrodes of the secondary side in between the electrodes of the primary side or vice versa. A new configuration of interleaved electrodes was proposed and analyzed in a previous paper using models. In this paper, the experimental validation of its features is presented, showing that interleaving of electrodes improves not only PT performance but also the whole power converter. A 20 samples batch of this new PT design has been tested, including repeatability studies which are useful to analyze the manufacturing tolerances.**

I. INTRODUCTION

Piezoelectric Transformers (PTs) operation principle is the piezoelectric effect, which converts the electrical energy through mechanical vibration.

PT shape, type of piezoelectric material and its polarization direction determine the working vibration mode, by changing the way of transferring energy between primary and secondary side. A widely used PT structure is the Rosen-type [1], but the output power is limited to 4-5W, because at higher power level the efficiency of the PT decreases too much. Other widespread PT structure is a disc working in radial mode, patented by FACE electronics [2]. As the resonance frequency is inversely proportional to the dimension of vibration, thickness mode becomes feasible in order to work at higher frequencies. For example, NEC has patented a multilayer square plate working in thickness mode [3]-[5].

In this paper, the alternative suggested is a ring shaped PT, working in the first order of thickness mode. PT is made of the ceramic material Pz26 [6], because its high power capability (due to the high permittivity ε, because Power density $\propto \varepsilon \cdot f \cdot k_{eff}^2$, where f is the vibration frequency and k_{eff} is the electromechanical coupling coefficient). But this material exhibits a large electromechanical isotropy which induces the appearance of spurious modes (non desired vibration modes in different directions of the thickness one, which can exist in the proximity of the working frequency, disturbing the vibration, figure 1). A PT disc would be cheaper and simple to build than a ring, but there is no way to avoid the spurious modes in the design process. There exists the possibility to suppress the spurious modes in the working frequency range by selecting in a proper way the inner and outer diameters of the ring.

As it will be described in the next section, PT features are also improved when interleaving of the electrodes (that consists on placing the secondary electrodes between the primary ones or vice versa) is applied to a multilayer PT. It allows improving the converter features in terms of volume and radiated noise, since no magnetic components are needed to drive the PT because higher inductive behavior can be achieved with interleaved configuration of electrodes. In [7], a new configuration of interleaved electrodes was proposed and analyzed using models. In this paper, measurements with several real samples are presented, validating the advantages of this new interleaving configuration.

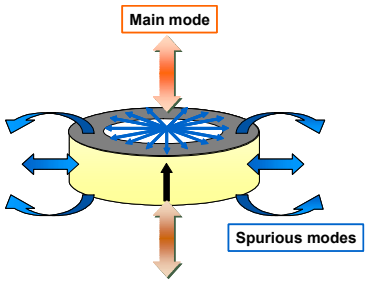

Figure 1. PT vibration modes.

II. INTERLEAVING CONCEPT AND ADVANTAGES

In conventional PTs (Figure 2.a) electrodes of primary side are separated from electrodes of secondary side. PTs interleaving structure modifies the electrode distribution, by placing the electrodes of one part of the PT in between the electrodes of the other part, as it is shown in figure 2.b (interleaving of Type I) and figure 2.c (interleaving of Type II).

Advantages of both types of interleaving have been analyzed in detail in [7]. The optimum waveform to drive a PT is a sinusoidal voltage but, **if the efficiency of the component is penalized by driving it with a squared voltage, the whole converter can be improved by suppressing the magnetic components**.

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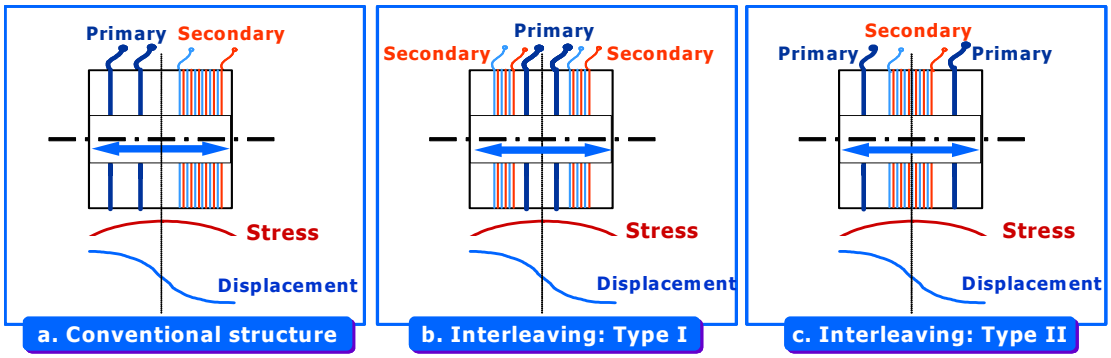

Figure 2. PT structures with different electrode distribution, working in thickness mode.

The following two features are essential to design a magnetic-less converter based on PTs:

- **Reduction of the high frequency vibration orders of the thickness mode**, due to the symmetry of the PT structure. These higher orders are spurious modes, which can affect PT performance if they are driven by the harmonic content of the squared input voltage.
- **Higher inductive behavior** (when the phase of the input impedance is positive), which makes feasible to achieve soft switching voltage transitions (ZVS). PT efficiency decreases due to the increment in the circulating energy. But the whole converter performance is improved as no magnetic component is needed to drive the PT.

Other important advantages of the interleaving of electrodes in PTs are:

- **Electromechanical conversion is increased** by improving the generation or reception of mechanical energy. The electromechanical coupling coefficient, defined in [8], as:

$$k_{eff}^2 = \frac{\text{Energy converted}}{\text{Input energy}}$$

is higher. This is possible by placing the electrodes in the maximum stress zone, which for our physical conditions is in the middle of the device (as can be deduced from the stress representation shown in figure 2).

- **PTs with interleaving admit higher variations on the input voltage.**

Interleaving of Type II has two additional advantages:

- **No isolation layer of inactive material is needed**, because the position of electrodes allows primary to behave also as isolation layer. This feature improves k_{eff} and efficiency of the PTs.
- **Input breakdown voltage will be higher,** as the distance between primary electrodes is larger. One of the limitations in PTs performance is the maximum electric field that can be applied to the piezoelectric material (2kV/mm) [6]. Therefore, the thicker the primary layer the higher input voltage can be.

III. DESCRIPTION OF THE PTS SAMPLES

Type I and Type II PTs, shown in figure 3, have been designed for the same application, a mobile phone AC adapter (universal input voltage, output voltage is 12V and output power is 10W), since it allows to compare both structures in a proper way. It is not the objective of this paper to describe the design process of the PTs, but its experimental validation. The design method is described in detail in [9] and combines results of analytical one dimensional models and results of Finite Element Analysis tools, which takes into account two/three dimensional effects.

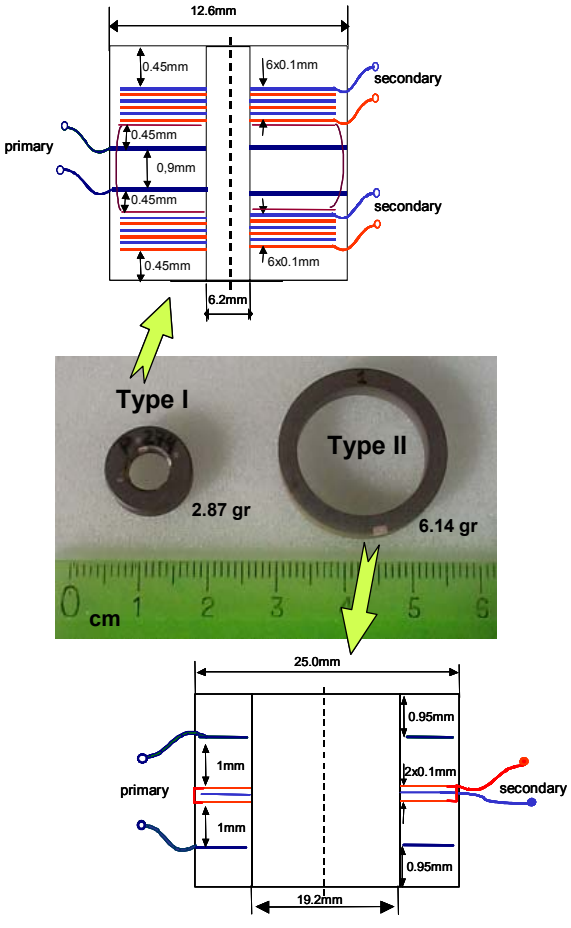

Figure 3. PTs of Type I and Type I.

PT of Type I has four electrodes in the primary side and the secondary side contains twelve electrodes split into two groups of six electrodes at both sides of primary. PT of Type II has two electrodes in the secondary side and the primary contains one at each side. Thickness is the same for both PTs (around 4 mm). Electrode area is 69mm^2 for Type I and 200mm^2 for Type II. Type II is designed to improve the Type I results in terms of cost (by reducing the electrode number) and to obtain the higher input voltage variation and ZVS in the whole frequency operating range, more than in size terms. From sensitivity analyses done in [10], it can be deduced that increasing the area helps to obtain the electrical PT requirements.

IV. EXPERIMENTAL VALIDATION

Measurement results of the new Type II PT design are presented in this section. Small signal measurements, driving sinusoidally the PT with a very low amplitude waveform, are detailed in subsection A. In subsection B, large signal measurements are done, driving the PT not only with sinusoidal voltage but also with square voltage. Finally in subsection C, some practical problems found during the experimental measurements are presented.

All these measurements will be also compared with the results of Type I PT presented in [7]. In that paper, it was demonstrated that interleaving of Type I improves the PT conventional structure.

Besides that, a repeatability study has been done with the 20 samples batch of Type II PT to validate the manufacturing process and the tolerances (in dimensions and material properties), considering their influence on the PT performance.

A. Small Signal Test Results

Small signal measurements, including the input impedance at different load conditions, are required in order to calculate the k_{eff} and to look for non-desired spurious modes. The input impedance magnitude of both samples under open circuit conditions is shown in figure 4, validating the reduction of the high frequency vibration orders of thickness mode with Type II design. This is a good design because **k_{eff} is very high (~50%)** and the **working frequency range** (between resonance frequency, fres, and antiresonance frequency, fares) **is clean of spurious modes**.

Besides that, the input impedance magnitude and phase have been measured with the optimum load, which is the one that maximizes the efficiency of the PT (12.7 Ω, in this case). These measurements are shown in figure 5 (for Type I PT) and figure 6 (for Type II PT). Maximum impedance phase under the optimum load conditions is higher with PT of Type II (~75º) than with PT of Type I (~59º). The higher the inductive behavior the higher the ZVS capability, then **Type II PT has higher ZVS capability**.

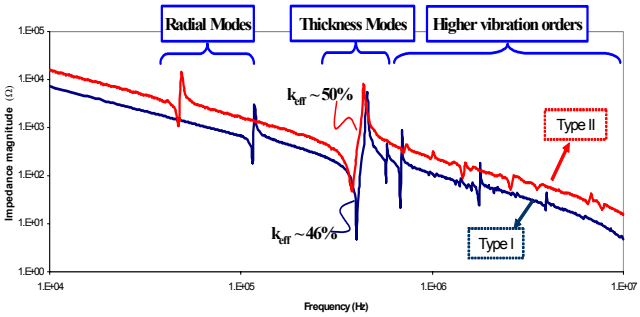

Figure 4. Harmonic analysis. Frequency response of input impedance for both interleaving types.

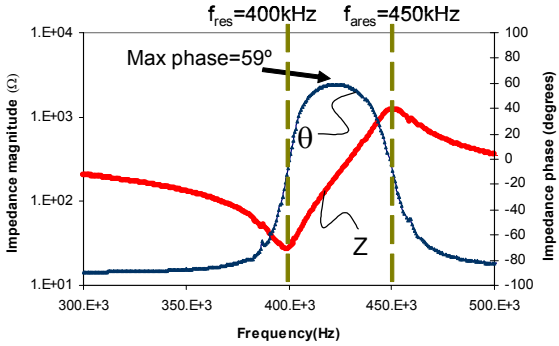

Figure 5. Type I PT input impedance magnitude (Z) and phase (θ) around resonance.

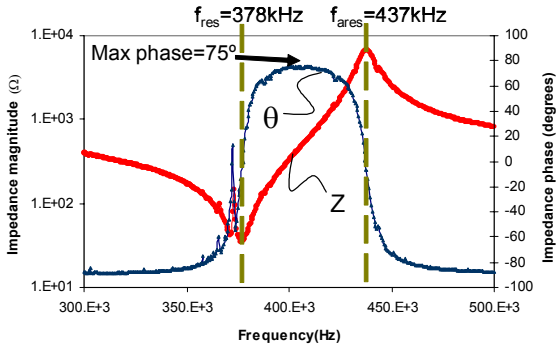

Figure 6. Type II PT input impedance magnitude (Z) and phase (θ) around resonance.

Small signal test is also useful to make a repeatability study of the batch, that has been manufactured in a carefully, very controlled and non automatic process. The objective is to obtain the real manufacturing tolerances to be compared with the "theoretical" manufacturing tolerances [6]. Manufacturing tolerances, in the dimensions and in the material properties too, have influence on the PT performance. One of the problems during the design stage is taking them into account in order to obtain a design in which the tolerances do not induce changes on the PT electrical performance. For example, spurious modes are very sensitive to the diameter selection ([9]) and it is not easy to find an inner and outer diameter, clean of spurious modes inside the tolerance margin.

TABLE I.
REPEATABILITY STUDY. INPUT IMPEDANCE FROM PRIMARY SIDE UNDER NO LOAD CONDITIONS.

Number of the Sample	1	2	3	4	5	6	7	8	9	10	Max	Min	Avg	σ
fres (kHz)	380.9	380.0	380.9	382.9	380.4	381.9	380.0	383.8	382.9	385.3	385.3	380.0	381.9	1.8
fares (kHz)	440.6	441.8	444.0	444.6	440.1	442.9	442.9	445.1	442.3	447.4	447.4	440.1	443.2	2.2
k_{eff} (%)	50.25	51.01	51.38	50.82	50.26	50.64	51.38	50.64	50.07	50.83	51.38	50.07	50.73	0.5
|Z| fres (Ω)	3.56	3.32	3.25	2.81	3.16	3.21	2.64	5.27	4.12	4.27	5.27	2.64	3.56	0.8
|Z|fares (kΩ)	41.49	89.87	115.13	49.37	37.12	7.21	154.27	36.53	47.12	43.41	154.27	7.21	62.15	44.1
Max θ	88.6	89.3	89.1	88.8	88.6	89.0	89.4	88.7	88.7	88.7	89.4	88.6	88.9	0.3

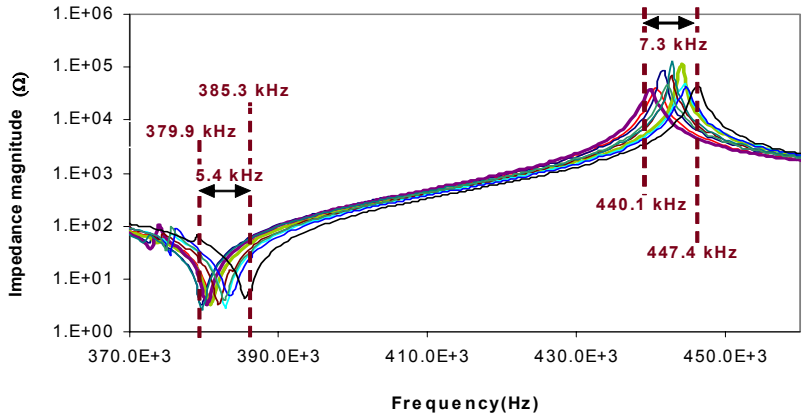

Figure 7. Input impedance vs frequency of the good samples under no load conditions.

From the 20 samples batch, 10 samples have been selected in order to be considered in the repeatability study. Results of the input impedance under no load conditions have been summarized in Table I and figure 7. Resonance and antiresonance frequency of all the samples is very similar and, in consequence, k_{eff} too. The bigger differences are in the input impedance at antiresonance frequency ($|Z|f_{ares}$). The reason is that this value not only depends on the PT properties but in the experimental set-up used for the measurements. The test has been done without soldering the wires to the PT electrodes, only putting them in contact, in order to avoid the influence of a bad soldering. It is not easy to ensure the same electrode-wire contact for all the samples.

From these results it can be concluded that repeatability is good considering that this is the first manufacturing batch for PT Type II and that some technical problems have arisen during the manufacturing process (it has not been possible to polarize entirely the secondary side). Actual manufacturing tolerances measured in the same batch samples are smaller than the expected "theoretical" tolerances given by the manufacturer ("theoretical" tolerances are about ±3% for the thickness of each layer and the inner and outer diameters). Its influence on the PT performance has been analyzed in [9]. Therefore PTs design and manufacturing process is carried out successfully with feasible and good quality PTs samples to be integrated in the converter.

B. Large Signal Test Results

PTs have been mounted in a PCB and driven in two different ways: with a sinusoidal waveform, as it is shown in figure 8, and with a square waveform, as it is shown in figure 9. First of all, PT is tested under a sinusoidally input voltage, which is the one that optimizes the PT performance. But the objective is to optimize the whole converter avoiding magnetic components at the PT input. Therefore the PT can also be driven with a square voltage waveform, keeping the efficiency good enough for the application.

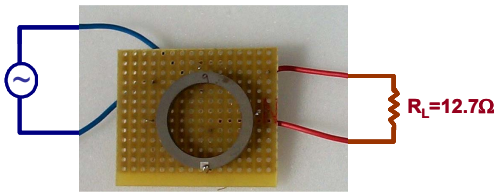

Figure 8. PT large signal test (sinusoidally voltage driven).

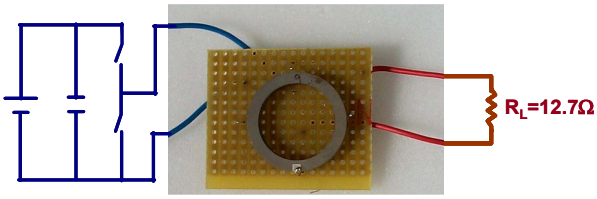

Figure 9. PT large signal test (squared voltage driven).

When the PT is sinusoidally driven, the objective is to study the PT efficiency and power capability, under the optimum load condition. As seen in figure 10, efficiency of Type II PT is lower due of its higher inductive behavior

(that implies more circulating energy). Nevertheless, it is still high enough for the application because **it has been possible to extract the almost 10W required**, with this first batch (Figure 11). Besides, the lack of total polarization of the secondary side is reducing the efficiency too.

Type II PT has higher breakdown input voltage, because its primary layer is thicker and presents the same input voltage variation than Type I, considering a smaller frequency range (Figure 12).

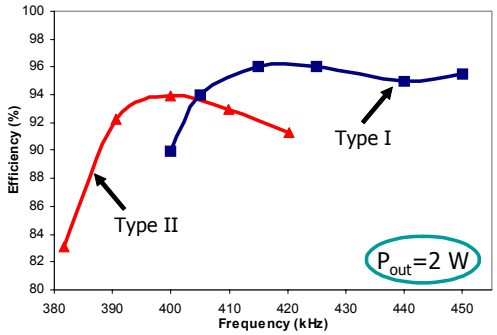

Figure 10. Sinusoidal test: PT efficiency vs frequency.

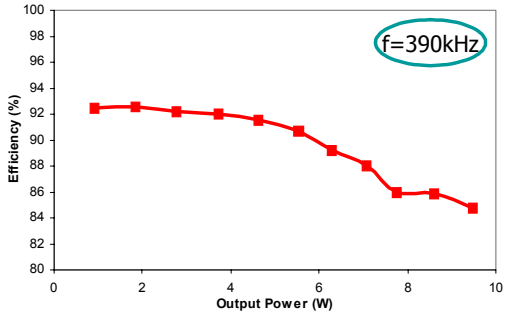

Figure 11. Sinusoidal test: Type II PT efficiency vs input power.

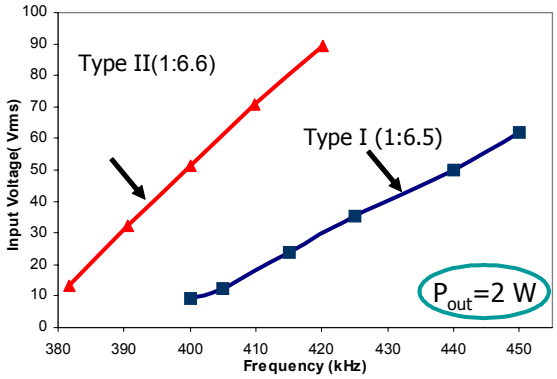

Figure 12. Sinusoidal test: PT input voltage vs frequency.

Figure 13 shows the input voltage and current of the Type II PT. As the **phase shift between both waveforms is about 71º**, the inductive behavior of the PT is very high and ZVS is achieved in the whole input voltage range, as it is shown below by driving the PT with a square voltage.

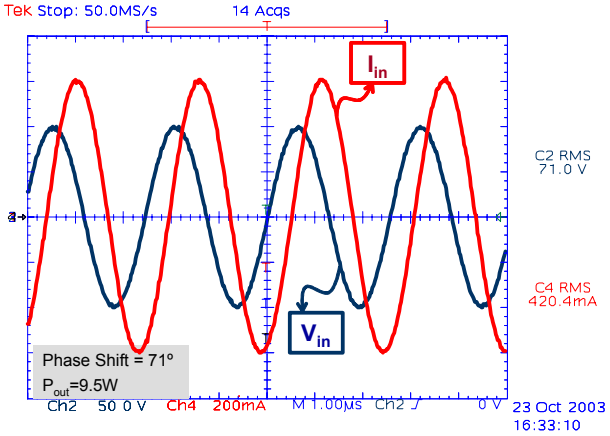

Figure 13. Type II PT input waveforms, driven with a sinusoidal voltage.

When the PT is driven with a square voltage, the efficiency decreases, as it was expected: efficiency at full load is 85% with a sinusoidal voltage and 80% with a square voltage. Nevertheless, **ZVS is achieved**, as shown in figure 14. It is also important to highlight that the PT presents ZVS not only at full load conditions but also at low load conditions. This is illustrated in figure 15, where PT is tested under a 25% of the load.

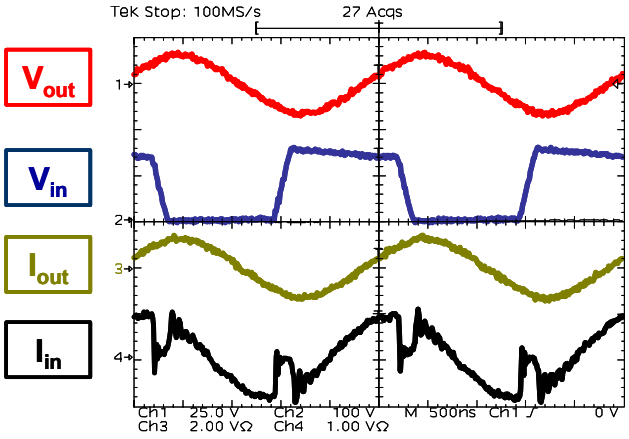

Figure 14. Type II PT waveforms, driven with a square voltage. P_{out}=10W. Full load conditions.

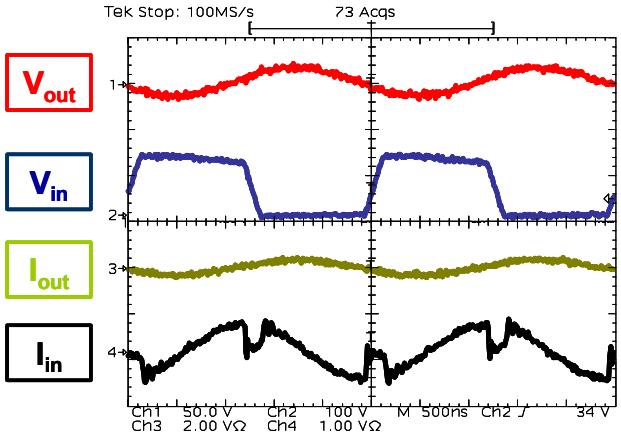

Figure 15. Type II PT waveforms, driven with a square voltage. P_{out}=2.5W. Low load conditions.

PT design has been validated to work in a magnetic-less converter like the one shown in figure 16. The topology is selected according to the application and to the PT driving way, that is the input voltage waveform applied to the PT. For this particular example, a Half-Bridge is selected because it is widely used with PTs to generate the square voltage for this input voltage range and power level. The rectifier stage selected is a full bridge because no magnetic components are needed.

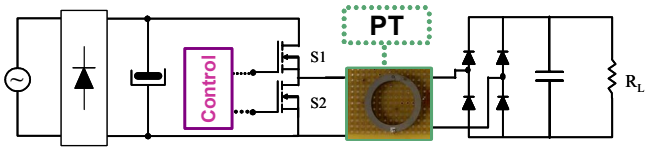

Figure 16. Suitable power topology for the magnetic-less converter.

C. *Practical problems*

If PT is kept during a long time in high losses conditions, its temperature will rise causing a degradation of the PT material and electrodes. Some of the solders can be broken too. A detail of the electrodes and the solders is shown in figure 17 and figure 18 respectively.

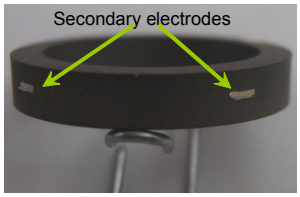

Figure 17. Type II PT electrodes.

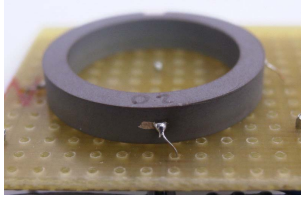

Figure 18. Type II PT solder.

Figure 19 shows a comparison of the input impedance of the PT just carefully soldered and the input impedance of the same PT after having been tested in large signal and high losses conditions (degraded PT). When the PT is degraded, several spurious modes appear, k_{eff} decreases and, according to this, the power density of the PT drops.

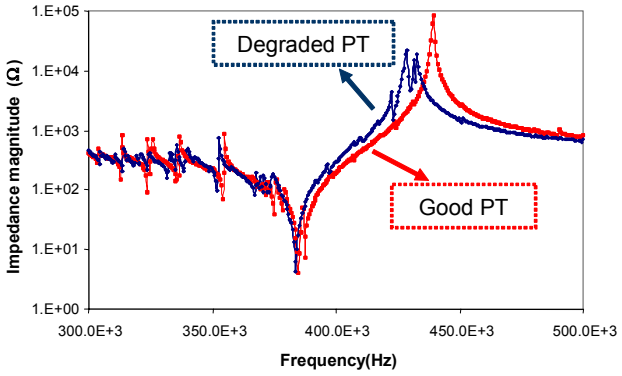

Figure 19. Degradation influence on the Type II PT input impedance.

V. CONCLUSIONS

PT design with a new interleaving structure (Type II) has been validated. The new Type II PT design improves the previous Type I interleaving structure in two main aspects:

- Higher breakdown input voltage.
- Lower cost, since the same electrical requirements are fulfilled with less number of electrodes.

More features of this Type II PT design are:

- Suppression of the high frequency vibration orders.
- Working frequency range clean of spurious modes and higher k_{eff} (>50%).
- Higher inductive behavior and so, higher ZVS capability. In fact, PT design has been optimized in order to achieve ZVS in a wide input voltage range.
- Higher variations of the input voltage.

Repeatability studies have been useful to deduce that the real manufacturing tolerances are not as important as it was expected, comparing with the "theoretical" ones (given by the manufacturer). Electrical performance of the PTs from the same batch is very similar.

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Comparison of different alternatives to drive Piezoelectric Transformers

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***Abstract*- Usually, the performance of Piezoelectric Transformers (PTs) is optimum when they are sinusoidally driven. The PT can also be driven with a quasi-square voltage waveform. Although PT performance is not optimized with a squared driving, corresponding topologies can be simpler and the whole converter can be improved. Those alternatives that keep an interesting trade-off between complexity and PT efficiency are compared, helping to select the best approach for different applications*.**

I. INTRODUCTION

Piezoelectric Transformers (PT) are becoming an alternative to magnetic transformer in some particular applications where the size and the weight of the power converter are critical issues. The main features of these devices are high power density, high isolation levels and low EMI content. These characteristics make PTs very attractive for low power DC/DC or AC/DC converters ([1] and [2]).

The performance of a PT strongly depends on how the PT is driven, being usually the optimum way applying a sinusoidal waveform. Depending on the applications, the needed networks to drive sinusoidally the PT can be very complex. Driving a PT with a quasi-square voltage is also possible. Although this solution is not the optimum from the PT point of view, it can allow for simpler networks, keeping the PT efficiency good enough. Several works have been published related on how a PT can be driven ([3] and [4]). In this paper it is analyze and compare those alternatives that keep an interesting trade-off between complexity and PT efficiency. Advantages and drawbacks are studied, helping to select the best approach for different applications.

II. PIEZOELECTRIC TRANSFORMER DESIGN

Two different PT samples with two different designs have been considered to develope the analysis. The small signal test of the corresponding samples is shown in Figure 1. Both samples work in the first order of thickness vibration mode. The operating frequency range is located between resonance (f_{res}) and antiresonance (f_{ares}) frequency.

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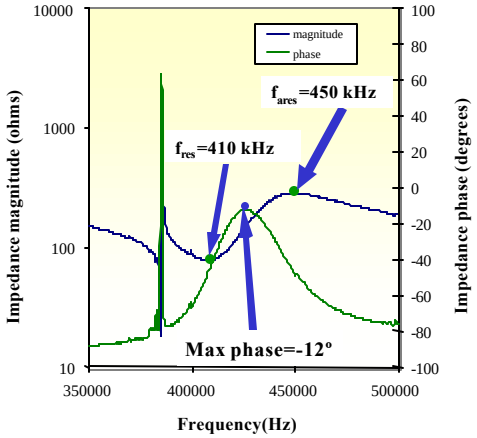
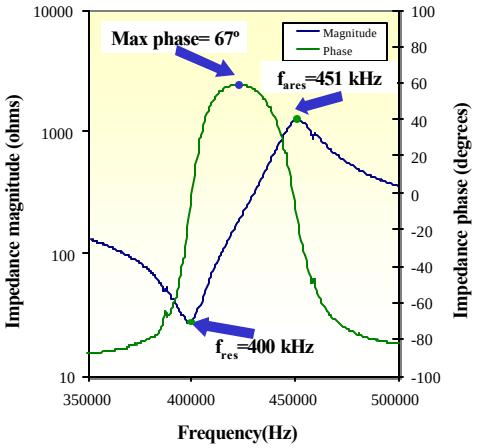


Sample A. Bad inductive behavior



Sample B. Good inductive behavior

Figure 1. Magnitude and phase of the input impedance measured in Sample A and Sample B with their corresponding resistive loads.

The measured electrical features of each sample with its optimum load (R_{opt}) are summarized in Table I. The different geometry of the samples makes that the electrical performance of both samples is different. The operating frequencies of both samples are very similar. The main differences between both samples are the inductive behavior in the operating frequency range and the electromechanical coupling coefficient (k_{eff}).

TABLE I

ELECTRICAL FEATURES OF THE SAMPLES

Sample	fres (kHz)	fares (kHz)	Ropt ( )	keff (%)	Vin range	Maximum phase (degrees)	PT efficiency (%)
A	410	451	7.5	41	2	-12	97
B	400	451	5	46	3	67	96

The inductive behavior of the PT, related to its input impedance phase, can provide Zero Voltage Switching (ZVS) condition if the PT is driven with a square voltage. High k_{eff} allows working in a wider frequency range as well as wider input voltage variation (V_{in} range), since it is related with the distance between resonance and antiresonance frequency

$$k_{eff} = \sqrt{\frac{f_{ares}^2 - f_{res}^2}{f_{ares}^2}} \qquad (1)$$

As seen in Table I, the input impedance phase of Sample B is higher than the one of Sample A. Therefore, Sample B has been designed with good inductive behavior to provide ZVS. In addition to this, Sample B allows for wider input voltage range since the value of k_{eff} is higher.

III. CONSIDERED ALTERNATIVES TO DRIVE PIEZOELECTRIC TRANSFORMERS

All the analyzed alternatives are based on the Half-Bridge (HB) topology plus and input matching network (Figure 2). The HB stage generates a square voltage (V_{AB}), however this hard-square voltage can not be applied directly to the PT. The PT should be driven sinusoidally or with a soft-square voltage. The main goal of the input matching network, placed between the HB stage and the PT is to provide and inductive behavior to achieve ZVS in the HB switches and, overall, to drive softly the PT. The input impedance (Zin) seen by the HB stage becomes a very important parameter to design properly the converter, in particular, $_{in}$ and G_{in} are the key parameters:

q_{in}: input impedance phase, accounts for the inductive behavior.

G_{in}: input conductance (real part of the input admittance), accounts for the power that can be transferred for a given input voltage [5] as it is shown in equation (2).

$$P_{in} = G_{in} * V_{in}^2 \qquad (2)$$

Three different structures of the input matching network are compared in this paper (Figure 3): series inductor, parallel inductor and magnetic-less.

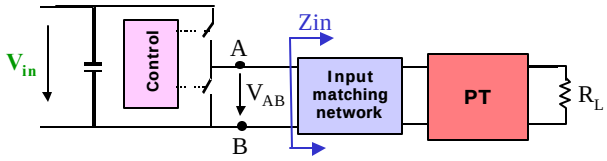


Figure 2. Considered converter topology

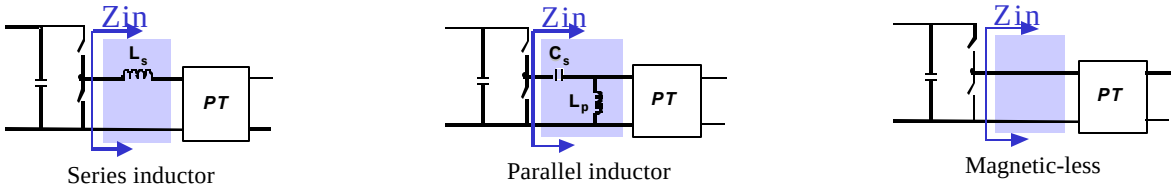
It is important to highlight that the aim of this paper is to improve the whole converter, hence only the simplest structures for the input impedance matching network have been considered. Depending on the input impedance of the PT ($_{PT}$ and G_{PT}), the needed matching network will be more or less complex. Since the analysis is focused on the PT input matching network, the output rectifier has been substituted by an equivalent resistive load.

IV. SERIES INDUCTOR

This structure drives the PT sinusoidally, optimizing the PT efficiency. A minimum value of the inductance is necessary to make sinusoidal the PT input voltage. The main characteristics of this topology are detailed below.

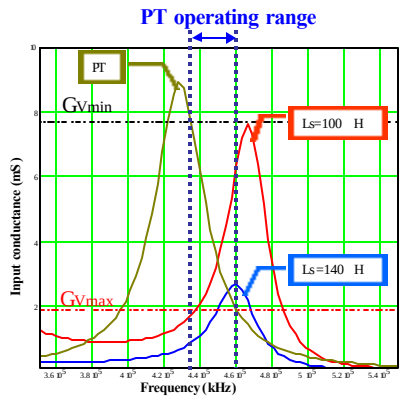
A. Restricted design

Series inductor affects $_{in}$ as well as the G_{in}. Input conductance of sample A varies between 10.3 mS (G_{Vmin}) and 2.4 mS (G_{Vmax}) within PT operating range. Driving the PT directly with the HB stage, the input voltage range would be 52Vdc-107Vdc if the power transferred by the PT is 5W. However, when a series inductance is used to achieve soft waveforms in the PT, the G_{in} is modified.

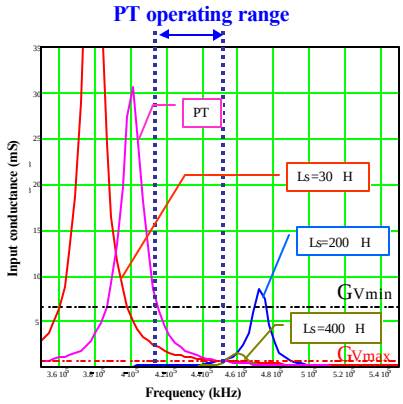


Series inductor Parallel inductor Magnetic-less

Figure 3. Considered alternatives to drive PTs.



Sample A



Sample B

Figure 4. Series inductor design with Mason model of the PTs.

As seen in Figure 4, a proper value for the inductance is around 100 H because it allows fulfilling the power requirements as well as to improve the inductive behavior of the input impedance. Taking into account (2), for the considered power (5W), the input voltage range achieved with series inductance (Ls=100 H) is 1:1.8 (87Vdc-154Vdc) which is slightly smaller than PT range 1:2 (52Vdc-107Vdc). Other values of series inductance as 140 H improve the inductive behavior but it does not fulfill the power and input voltage range specified.

The variation of input conductance (G_{PT}) for sample B is between 6.5 mS (G_{Vmin}) and 0.75 mS (G_{Vmax}). Therefore, driving the PT directly with HB stage, the input voltage variation between 50Vdc-147Vdc to transfer an output power of 3W. Figure 4 shows that it is not possible to find a value of the series inductance that guarantees sinusoidal voltage in the PT and at the same time satisfies the required input conductance, since G_{in} is strongly reduced by the L_s.

Series inductor allows for high PT efficiency by applying sinusoidal input voltage, nevertheless the applicability of the PT is restricted by series inductance value.

It has been measured Sample A with a series inductance of 120 H and its optimum resistive load at the output. As seen in Figure 5, the input PT voltage ($V_{IN,PT}$) is sinusoidal and the drain source voltage of the MOSFET (V_{AB}) has ZVS condition.

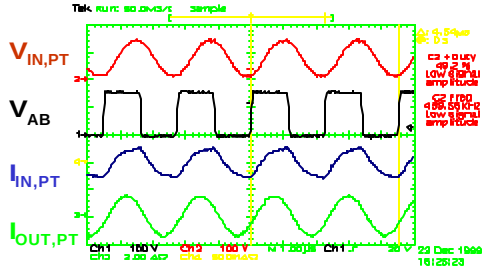


Figure 5. Measured waveforms with series inductance. Sample A.

(L_s=120 H, R_L=7.5)

Time(1 s/div), $V_{IN,PT}$(100V/div), V_{AB}(100V/div), $I_{IN,PT}$(500mA/div), $I_{OUT,PT}$(2A/div),

B. *Control Law*

As seen in Figure 4, depending on the value of the series inductance the control law changes. PT control law implies an increment of the switching frequency when there is an increment of the input voltage. By adding a series inductance of 100 H to the input of Sample A, the input conductance changes as well as the control law. That means, the higher the input voltage the lower the frequency. Besides, the maximum operating frequency is limited by the change of the control law.

C. *Input voltage range*

As aforementioned, it is not always possible to find a series inductance value for Sample B that fulfills the power and input voltage requirements. The reason for that is the variation of the input conductance (G_{in}). In order to fulfill power specifications, the value of the input voltage range can not be the desired one. In the case of Sample B, the smallest L_s value that guarantees sinusoidal voltage in the PT is 30 H. This value of L_s implies a reduction of the input voltage range from 1:3 (50Vdc-147Vdc) to 1:1.7 (87Vdc-147Vdc).

D. *Circulating energy*

The series inductor affects the input impedance phase (in) as it is shown in Figure 6, hence there is an increment of the circulating energy that affects the efficiency of the converter and allows for ZVS condition of the Half-Bridge stage.

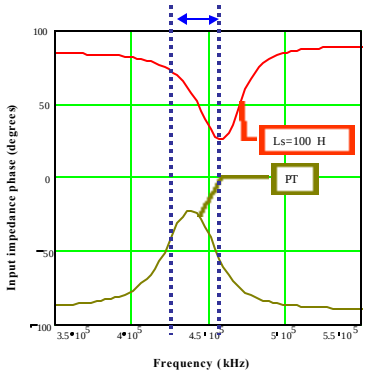


Figure 6. Influence of series inductance on input impedance phase. Sample A

Figure 7 shows the overall efficiency of the converter with series inductance for different output loads with Sample A.

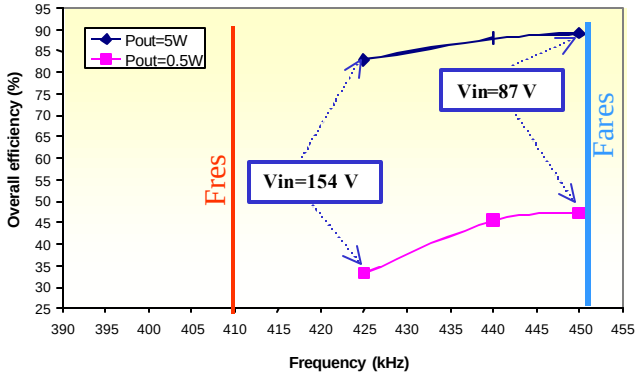


Figure 7. Converter efficiency measured with series inductance. Sample A
(L_s=100 H, R_L=7.5)

A more detailed information of the operating points 154V (5W and 0.5W) and 87V (5W and 0.5W) is shown in Table II and Table III respectively. The influence of the circulating energy is analyzed by comparing these tables. At high input voltage (Table II) the inductor current is very similar at 5W and 0.5W since input impedance phase is high (around 80 degrees) at these frequencies (425 kHz). This high input impedance phase produces bigger circulating energy, worsening the efficiency.

However, at low input voltage (Table III) when the operating frequency is higher (450 kHz), the influence of the series inductance on input impedance phase is smaller. Hence, the inductor current at 0.5W is five times smaller than it is at 5W since the circulating energy is smaller, increasing the efficiency.

E. Subharmonic driving

Subharmonic driving consists on applying a square waveform to the PT whose frequency is lower (usually 3 times) than the PT resonance frequency.

Because of the sinusoidal voltage at the input of the PT, the subharmonic driving concept can not be applied [6]. Therefore compact integrated circuit including MOSFETs and drivers can not be used when PT frequency is so high.

V. PARALLEL INDUCTOR

A series capacitor (C_s) and an inductor paralleled (L_p) to the PT form this structure (Figure 3). C_s is designed to eliminate average value of the input voltage in the PT and its impedance does not affect the input conductance in the operating frequency range. Therefore, this structure does not affect the input conductance of the PT (G_{in} G_{PT}).

A. Degree of freedom in the design

The value of the L_p only modifies the input impedance phase ($_{in}$) but does not affect the input conductance (G_{in}). Hence, there is a degree of freedom in the inductance value design. Parallel inductor has been designed for the same power and input voltage requirements that with series inductor.

TABLE II

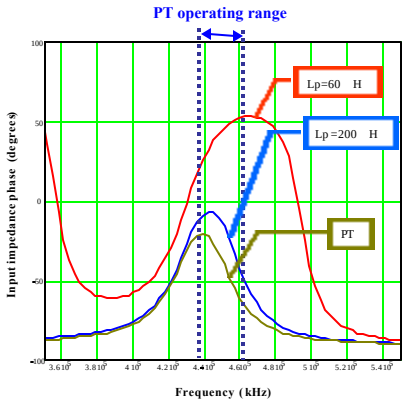
LOAD REGULATION WITH LS=100 H. EXPERIMENTAL RESULTS WITH SAMPLE A. VIN = 154 V

Resistive load ( )	Frequency (kHz)	Turn-on voltage (V)	$_{in}$ (degrees)	P_{out} (W)	HB efficiency (%)	IL_{max} (A)	$_{PT}$ (%)	$_{0}$ (%)
7.5	425	0	71	5	86	0.364	96	83
70.6	425	0	87	0.5	44	0.360	75	33

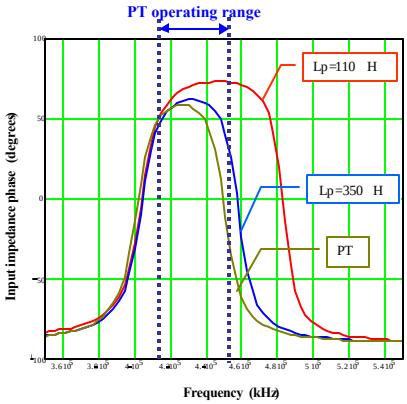
TABLE III

LOAD REGULATION WITH LS=100 H. EXPERIMENTAL RESULTS WITH SAMPLE A. VIN = 87 V

Resistive load ( )	Frequency (kHz)	Turn-on voltage (V)	$_{in}$ (degrees)	P_{out} (W)	HB efficiency (%)	IL_{max} (A)	$_{PT}$ (%)	$_{0}$ (%)
7.5	450	0	23	5	93	0.191	96	89
70.6	450	0	12.4	0.5	60	0.037	79	47



Sample A



Sample B

Figure 8. Parallel inductor design with Mason model of the PTs.

The minimum value of the inductance is selected taking into account that the resonance frequency of series capacitor and parallel inductance is far enough from the working frequency range. As it is shown in Figure 8, Sample A requires an inductance of at least 60 H in order to improve the inductive behavior of the input impedance seen by the HB and to provide ZVS condition at the input of the PT.

It has been measured Sample A with a parallel inductance of 70 H and its optimum resistive load at the output. As seen in Figure 9, the input PT voltage ($V_{IN,PT}$) is squared voltage with soft transitions.

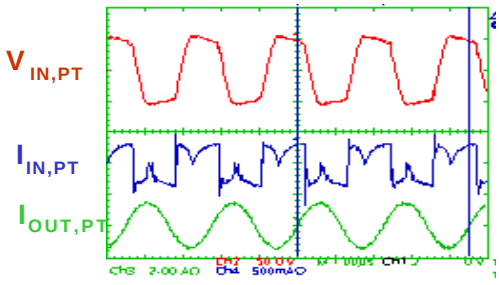


Figure 9. Measured waveforms with parallel inductance. Sample A.
(C_s = 33 nF, L_p=70 H, R_L=7.5)
Time (1 s/div) $V_{IN,PT}$(50V/div), $I_{IN,PT}$(500mA/div), $I_{OUT,PT}$(2A/div),

Because the input conductance is not affected, there are two features that are not modified respect to the PT ones:

Control Law

Input voltage range

B. *Circulating energy*

Parallel inductor affects the input impedance phase ($_{in}$), hence there is an increment of the circulating currents that affects the efficiency of the converter and allows for ZVS condition in the PT and switches. Since the inductor is connected in parallel, its current keeps constant. Hence, circulating current keeps almost the same at low load (0.5 W) than at high load (5 W), worsening the converter efficiency at low load.

Figure 10 represents the measured converter efficiency with parallel inductance at 5W and 0.5W with Sample A. It shows how circulating energy reduces the efficiency at low load for the whole input voltage range. Therefore, series inductance matching network produce less circulating energy than parallel inductor with Sample A (bad inductive behavior).

Table III and Table IV show both matching networks at the same operating conditions (input voltage and frequency). As seen in the table data the converter efficiency at low load is smaller with L_p than with L_s for Sample A.

TABLE IV

LOAD REGULATION WITH PARALLEL INDUCTANCE . SAMPLE A. EXPERIMENTAL RESULTS WITH CS= 33 NF AND LP=60 H. VIN = 92 V

Resistive load ( )	Frequency (kHz)	Turn-on voltage (V)	$_{in}$ (degrees)	P_{out} (W)	IL_{max} (A)	HB efficiency (%)	$_{PT}$ (%)	$_{0}$ (%)
7.5	450	0	52	5	0.36	94	91	85
136	450	0	85	0.5	0.4	65	42	27

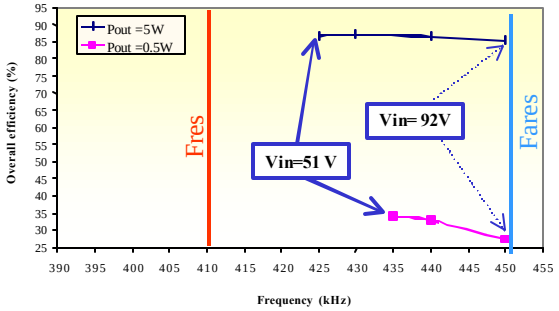


Figure 10. Converter efficiency measured with parallel inductance. Sample A. (Cs = 33 nF, Lp=60 H, RL=7.5)

Figure 11 shows the measured converter efficiency with Sample B. As parallel inductance does not affect the input impedance phase, it is always possible to find a value of parallel inductor to built the converter. Otherwise, series inductance does not allow achieving the specifications with Sample B.

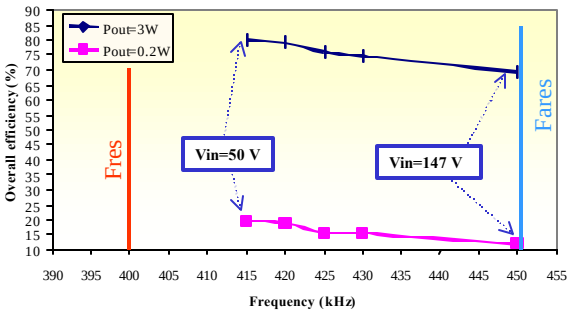


Figure 11. Converter efficiency measured with parallel inductance. Sample B .(Cs = 33 nF, Lp=110 H, RL=5)

C. *Subharmonic driving*

Because of the squared voltage at the input of the PT, the subharmonic driving concept can be applied [6] and compact integrated circuit for MOSFETs and drivers can be used. Therefore, the size of the converter can be reduced.

The study of this feature is not the aim of this work. Hence, there are no measurements in order to evaluate this aspect.

VI. MAGNETIC-LESS

This structure (Figure 3) allows avoiding the use of magnetic components so the PT must be designed to supply ZVS condition.

A. *Design PT for ZVS*

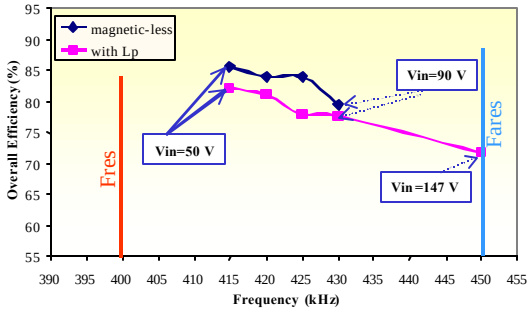
The input impedance phase ($_{in}$) is the PT one, hence the PT must be designed for having inductive behavior. As mentioned in paragraph II, Sample B has been designed with good inductive behavior.

B. *Control Law*

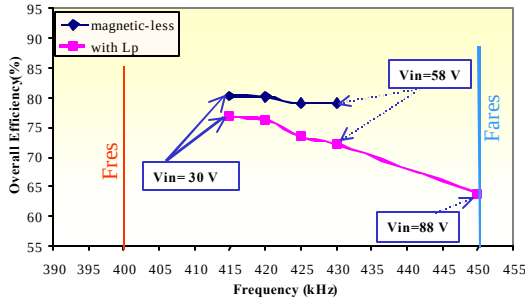
As any element is added at the input of the PT, the input conductance is the PT one. Hereby, the control law is not modified.

C. *Input voltage range*

Figure 12 compares the input voltage variation of magnetic-less and the parallel inductance topology for different output load. As can be seen in Figure 12, the magnetic-less topology reduces the input voltage range at both power levels (from 1:3 to 1:1.8). The operating range is reduced at that frequencies where the PT has an inductive behavior and is capable to provide ZVS condition, hence the input voltage range is reduced.



Pout=3W



Pout=1W

Figure 12. Efficiency comparison between parallel inductance and magnetic-less. Sample B (C_s = 33 nF, L_p=110 H, R_L=5)

By adding a small parallel inductor (Lp=350 H) input voltage range could be increased (from 1.84 to 2.5). As seen in Figure 8, this inductance value improves a little bit the inductive behavior increasing the input voltage range with a small increment of circulating energy.

The input voltage range can also be increased by allowing hard switching voltage transitions at the input of the PT.

Experimental data (Table **V** and Table VI) show that input voltage could be increased by the reduction of the PT

power capability due to the existence of hard switching transitions at the input of the PT (see VINPT in Figure 13 and Figure 14). Hard switching makes lower PT efficiency due to the peaks of the input PT current. However, there is a reduction of the power capability of the PT.

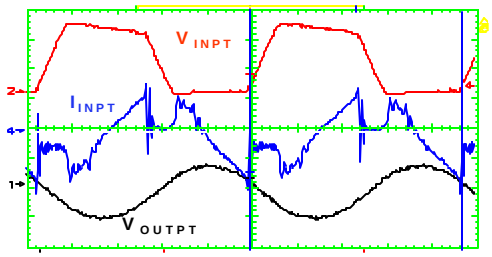


Figure 13. Magnetic-less measurements Sample B.Soft switching Time (500ns/div), $V_{IN,PT}$(10V/div), $I_{IN,PT}$(100mA/div), $V_{OUT,PT}$(2.5V/div),

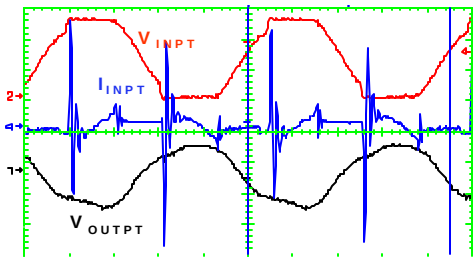


Figure 14. Magnetic-less measurements Sample B.Hard switching. Time (500ns/div), $V_{IN,PT}$(20V/div), $I_{IN,PT}$(200mA/div), $V_{OUT,PT}$(2.5V/div).

TABLE V

MEASUREMENT DATA WITH R=5 AND SOFT SWITCHING. MAGNETIC-LESS. SAMPLE B

Freq (kHz)	Vin (V)	Turn-on voltage (V)	Pout.(W)	$_{PT}$ (%)	$_{o}$ (%)
415	56	0	3	93	85.7
430	98	0	3	94	84

TABLE VI

MEASUREMENT DATA WITH R=5 AND HARD SWITCHING. MAGNETIC-LESS. SAMPLE B

Freq (kHz)	Vin(V)	Turn-on voltage (V)	Pout (W)	$_{PT}$ (%)	$_{o}$ (%)
405	19	7	1	94	75
435	75	12	1	92	70

D. *Circulating energy*

As said before, the higher the inductance values the lower the circulating current. Hence, the reduction even the elimination of the inductor improves the performance of the converter (size and efficiency). In Figure 12, it is shown how the efficiency of the converter is improved by avoiding the input inductor since the circulating energy is reduced.

E. *Subharmonic driving*

As mentioned before, the square driving allows using subharmonic driving control.

VII. CONCLUSIONS

Several alternatives to drive PT have been compared to determine which is the best solution for each application to improve the whole converter.

Series inductor allows driving sinusoidally the PT, obtaining the optimum performance of the PT with a simple matching network. However its design is restricted and it can not be applied in some applications.

Parallel inductor applies a soft-square voltage to the PT. There is a degree of freedom in the design of the converter and it does not restrict the applicability of the PT. Depending on the performance of the PT, the circulating energy can be reduced.

When the PT has bad inductive behavior (Sample A), series inductor is more appropriate than parallel inductor since circulating energy is smaller. If the PT has good inductive behavior (Sample B), parallel inductor becomes more interesting since input voltage range of the PT is not restricted and the energy handled by the inductor is small.

If the PT is designed with a good inductive behavior, the needed parallel inductor can be very small or even disappear. This magnetic-less concept makes more complex the design of the PT but it can provides a very competitive converter based on PT. Although the scope of the applicability of the PT is reduced, no magnetics are needed.

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Subharmonic Driving: a New Concept to Drive Piezoelectric Transformers in Power Converters

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Abstract- A new concept to drive Piezoelectric Transformers (PT) is presented and validated in this paper. The subharmonic driving consists on applying a voltage waveform to the PT whose fundamental frequency (f_{PT}/n) contains the resonance harmonic (f_{PT}) at which the PT transfers the energy. It is important to highlight that this solution is proposed in order to improve the whole converter, even if the PT performance is not as good as it could be with sinusoidal excitation. The PT should be specifically designed to handle more energy.

I. INTRODUCTION

Piezoelectric Transformers (PTs) present alternative characteristics to magnetic transformers, being an interesting solution in some particular applications [1]-[7]. Main advantages of PTs are high power density and high isolation levels with low EMI content. PTs are interesting in those applications where size, weight, isolation or high gain become critical specifications.

The design of a PT depends on many geometrical and constructive parameters such as area, length, material, shape, etc. The optimum operating frequency of the PT (f_{PT}) depends on its design. When the PT is electrically driven around this frequency (f_{PT}), it vibrates and transfers power to the secondary efficiently.

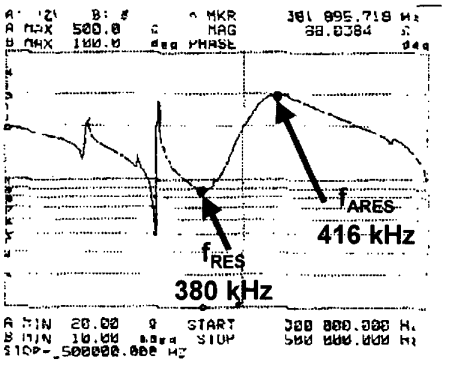


Fig. 1. Magnitude of the input impedance measured in the PT (*Sample A*)

Figure 1 shows the input impedance measured in a PT (*Sample A*). This PT works in thickness mode. The experimental results shown in the paper have been measured with this PT. It is a cylinder, its height is 4mm, the external diameter is 13 mm and the internal is 8mm. Optimum operating frequency of this PT (f_{PT}) is between its resonance frequency (f_{RES} = 380kHz) and its antiresonance frequency (f_{ARES} = 416kHz). The PT presents some spurious modes (figure 1) but the energy transfer has a very poor efficiency at these frequencies since the PT does not vibrate in the proper direction.

PTs are usually driven with a sinusoidal voltage waveform oscillating at the same frequency than the operating frequency of the PT (f_{PT}). Impedance matching networks ([3] and [6]) are used to generate this sinusoidal voltage, figure 2.

A new concept to drive Piezoelectric Transformers is presented in this paper. Topologies where this concept can be applied are studied and compared. This new concept is validated, showing actual measurements of a DC/DC power converter.

II. SUBHARMONIC DRIVING CONCEPT

The subharmonic driving consists on applying a voltage waveform to the PT whose fundamental frequency (f_{PT}/n) is lower than the operating frequency (f_{PT}) at which the PT transfers energy efficiently. This waveform should contain at least the operating harmonic of the PT (f_{PT}).

A easy way to achieve this condition is using a square waveform of frequency f/3 (fundamental harmonic). The PT can be designed to work at f, because the square waveform contains a third harmonic than can be used to drive the PT (figure 3).

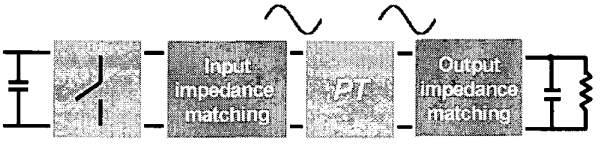


Fig. 2. Typical structure to drive sinusoidally a PT.

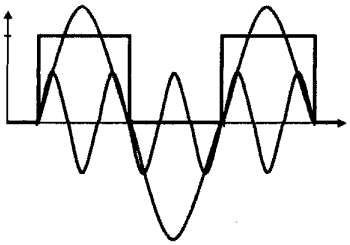


Fig. 3. First and third harmonic of a square waveform

This way, the switches used to generate the square waveform should work at frequency $f_{PT}/3$, which is three times lower than the operating frequency of the PT (f_{PT}). Main features of subharmonic driving are summarized below:

Advantages:

1) Size and weight of the PT is smaller because it is designed to operate at high frequency (f_{PT}) while switching frequency of the switches is three (or more) times lower ($f_{PT}/3$).
2) Compact commercial circuits that integrate the switches, the drivers and the controller can be used since switching frequency is low ($f_{PT}/3$).
3) If the PT is designed to show Zero Voltage Switching (ZVS), a small inductor is needed at the input of the PT, saving size and weight in the converter.

Drawbacks:

1) The PT handles more energy (circulating energy). The PT should be designed to handle circulating energy without heat transfer problems. The circulating energy usually produces an increment of size in the PT. However this increment is lower than the decrement caused by designing the PT to work at a frequency three times higher.
2) Dielectric losses are higher. The square voltage applied to the PT has to be three times higher with subharmonic driving ($f_{PT}/3$) than with normal driving (f_{PT}) to transfer the same amount of power. This higher voltage increases the dielectric losses if the PT is not specifically design to reduce these losses.

It is important to highlight that this solution is proposed in order to improve the whole converter, even if the PT performance is not as good as it could be with sinusoidal excitation.

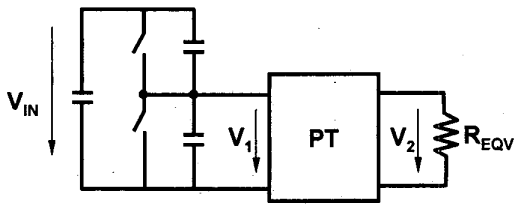


Fig. 4. Magnetic-less square driving topology

Goals in the design of the PT to apply the subharmonic driving are 1) to provide the maximum ZVS capability in the PT itself, 2) capability to handle circulating energy and 3) to reduce the dielectric losses.

III. TOPOLOGIES WHERE THE CONCEPT CAN BE APPLIED

One way to drive the PT with a subharmonic frequency is to apply a square voltage waveform to the transformer. Two topologies where this concept can be applied are the *magnetic-less square driving* (figure 4) and the *square driving with a parallel inductor* (figure 6).

A. Magnetic-less square driving

This is the simplest topology to drive the PT with a square waveform (figure 4). Obviously, the main advantage is its simplicity, only two switches are necessary. The switches are complementary driven with 50% duty cycle.

In this topology, ZVS condition depends exclusively on PT design. If ZVS is not achieved, switching losses in the PT as well as in the switches will be higher, limiting the applicability of this simple topology.

Figure 5 shows the current spikes measured at the input of a PT when there is no ZVS. When the PT is operating under no ZVS conditions its capability to transfer power is very limited since the PT heats up and the efficiency falls down. Therefore, this simple topology can be used if the PT is designed to provide ZVS condition.

B. Square driving with a parallel inductor

This topology is another option to apply square waveform to the PT (figure 6) and therefore subharmonic concept can be used. Main advantage of this topology, compared with the previous one, is that the parallel inductor allows for achieving ZVS. Hence, ZVS is not a restriction in the design of the PT.

The idea is to optimize the PT from the point of view of efficiency, circulating energy, dielectric losses, etc., achieving ZVS with a external parallel inductor. The capacitor and the parallel inductor increase the size of the whole converter.

To achieve ZVS with an external inductor benefits the PT design but increases the circulating current though the switches, reducing the efficiency of the power stage.

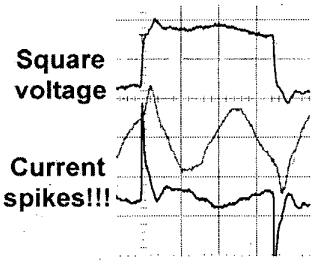


Fig. 5. Current spikes in a PT driven with a square voltage without ZVS

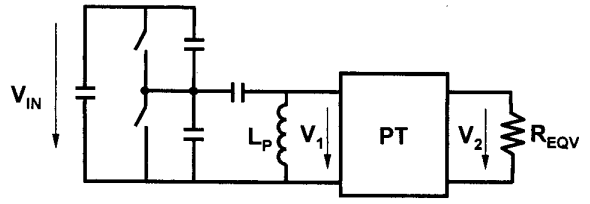


Fig. 6. Square driving with parallel inductor

Between these two topologies, the optimum design can be in a middle point. The PT can be designed with a certain amount of ZVS condition, keeping a high efficiency and small size. The rest of ZVS condition can be achieved by adding a small parallel inductor. The higher ZVS condition in the PT, the smaller the parallel inductor and the smaller the circulating energy through the switches.

IV. Design for Subharmonic Driving

As said above, important factors that should be regarded in the design of a PT for subharmonic driving are the ZVS capability, the capability to handle circulating energy and the dielectric losses. Of course, efficiency and size of the PT are the key goals.

ZVS capability is closely related with the capability of a PT to handle circulating energy. In fact, when a PT has good ZVS with good efficiency is because it has good capability to handle circulating energy. Figure 7 shows a simple equivalent circuit of a PT. The series resistance R_S represents the losses in the PT; a small value of R_S means a higher capability to handle circulating energy.

Figure 8 shows the voltage and current measured at the input of two different PTs (*Sample A* and *Sample B*) when they are sinusoidally driven.

Sample A is a PT with NO ZVS. Efficiency is high (97%) and the phase shift between current and voltage is –13° (capacitive behavior). The series resistance R_S is 2.3Ω.

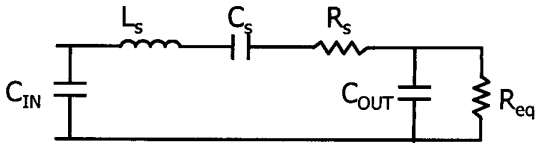


Fig. 7. Simple equivalent circuit of a PT.

Sample B is a PT designed for a similar application than *Sample A* but with good ZVS and good capability to handle energy. The phase shift is +54° (inductive behavior), hence it handles more circulating energy but the efficiency is still high (97%) because the series resistance is smaller (1.1Ω).

Figure 9 shows how the *Sample B* allows for *magnetic-less square driving* (figure 4) since it provides full ZVS. An important criterion to apply subharmonic driving is to design with a small R_S and good ZVS.

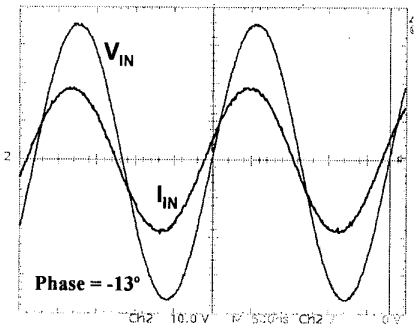
Dielectric losses are the other important aspect to be considered in the design of a PT for subharmonic driving. Dielectric losses depend mainly on the material and the input capacitance (C_{IN}). The material used is the PZT. The smaller the input capacitance, the lower the dielectric losses.

Applying these design criteria, two PTs are designed, one for subharmonic driving (*Design C*) and the other for normal driving (*Design D*). To optimize the design of the PT, a 1D model based on transmission lines has been used. This 1D model accounts for the dielectric losses.

The model of *Design C* (PT optimized for subharmonic concept) has been used to make simulations and evaluate its applicability. Results are promising, keeping a high efficiency (94%) when operates at $f_{PT}/3$. Its efficiency is 95.5% when operates at f_{PT} (Table I). This PT has good efficiency with subharmonic driving since it has good ZVS and capability to handle circulating energy as well as small dielectric losses.

However, the *Design D* behaves poorly when it is driving at $f_{PT}/3$. Efficiency of this PT model is 95% when operates at f_{PT}, however it is smaller 90% when operates at $f_{PT}/3$ (Table I).

***Sample A* (η = 97%, R_S = 2.3Ω)**



***Sample B* (η = 97%, R_S = 1.1Ω)**

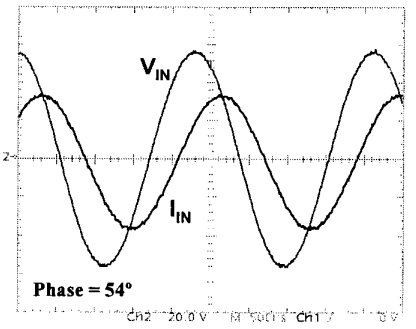


Fig. 8. Sinusoidal driving of *Sample A* and *Sample B*.

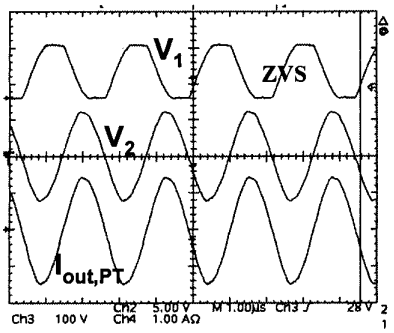


Fig. 9. Magnetic-less square driving topology with *Sample B*. Experimental results.

The penalty paid by designing for subharmonic concept (*Design C*) is the increment in the size, 20% bigger respect *Sample A*. However *Design C* woks from higher input voltage. Subharmonic concept could be an interesting idea in high input voltage applications.

TABLE I
SQUARE VOLTAGE APPLIED TO THE PT
SIMULATION RESULTS

	f_{PT}		$f_{PT}/3$	
	V_{IN} (V)	η(%)	V_{IN} (V)	η(%)
Model of *Design C*	185	95.5	555	94
Model of *Design D*	56	95	168	90

V. VALIDATION: EXPERIMENTAL RESULTS

Subharmonic driving concept has been tested and validated using the scheme of figure 6 with the *Sample A*. A parallel inductor is used to achieve ZVS. Figure 10 shows the measured waveforms. Frequency of the driving voltage V1 is $f_{PT}/3$ (130kHz), while PT is operating at f_{PT} (390kHz) as shown in the output voltage of the PT (V2). To analyze this new concept, the same PT is driven in three different ways:

1) *Sinusoidal driving at f_{PT}*: PT efficiency is 97% and the maximum power that can deliver is 12W.

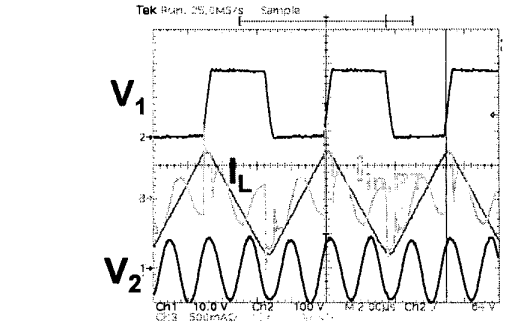
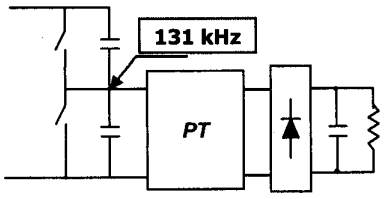


Fig. 10. Subharmonic driving validation: waveforms measured in the PT.

2) *Square driving with parallel inductor at f_{PT}*: PT efficiency is 96% and the maximum power that can deliver is 12W. Since ZVS condition is achieved (parallel inductor) there is almost no difference between sinusoidal driving and square driving at f_{PT} from the point of view of the PT.
3) *Square driving with parallel inductor at $f_{PT}/3$*: the PT efficiency is smaller than in the previous cases because there is more circulating energy and dielectric losses are higher. The PT works properly at 6W with 93% efficiency. If power is increased up to 8W, heat lowers the efficiency down to 90%.

This PT is designed to deliver 12W, but the heating caused by the circulating energy and the dielectric losses, limits down to 6W-7W the power transferred by this PT when subharmonic concept is used. These measurements are very interesting because they validate the new concept. Efficiency in the PT falls because the PT had not been designed for subharmonic driving.

This new driving concept has been tested in a simple DC/DC converter (figure 11). Oscillator, driver and switches are packaged in a commercial integrated circuit (IR51HD420). This integrated circuit can be used because it is operating at 130kHz while the PT is at 390kHz. As figure 11 shows, ZVS is not fully achieved since this PT had not been designed for this application and ZVS condition was not considered in its design.



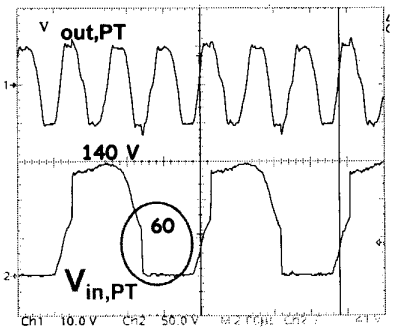


Fig.11. Subharmonic driving with magnetic-less solution. Experimental results..

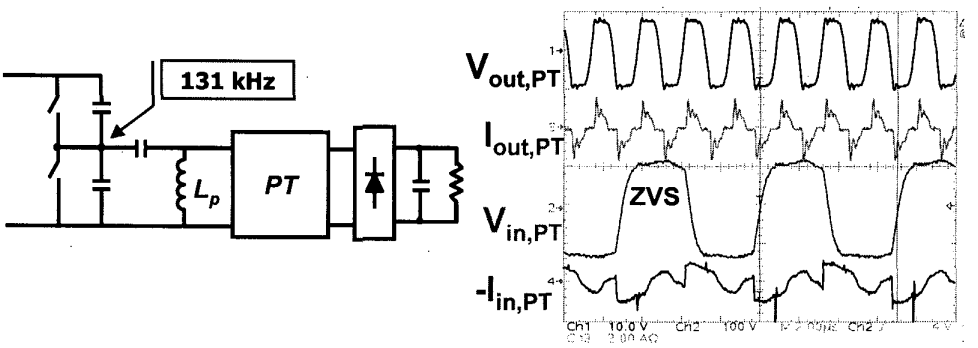


Fig. 12. Subharmonic driving with parallel inductor. Experimental results.

To achieve the ZVS condition, a parallel inductor is added to the previous converter. Experimental waveforms are shown in figure 12. Input voltage is 240V, output voltage is 7V and output power is 3W.

These measurements confirm that subharmonic driving works. It is a new concept that allows for low frequency in the switches while the PT is operating at high frequency.

VI. CONCLUSIONS

Subharmonic driving is a new concept to drive Piezoelectric Transformers that can optimize the size and weight of the whole converter. PT can be smaller because it operates at high frequency (f_{PT}) while switching frequency of the switches is three (or more) times lower ($f_{PT}/3$) allowing the use of compact commercial circuits that integrate the switches, the drivers and the oscillator.

Subharmonic driving penalized the size of the PT, compared with normal driving (f_{PT}), due to the heating caused by the circulating energy and the driving losses. The PT should be specifically designed to avoid the heating of the PT and achieve a high amount of ZVS condition to reduce as much as possible the size of the parallel inductor or even eliminate it.

This new concept has been validated in a DC/DC power converter with a PT never designed for this purpose. 6W are delivered by this PT with subharmonic driving.

Experimental and simulated results show that the concept works but further studies are necessary to find an application field for this new driving concept. For example, subharmonic driving could present advantages in high input voltage applications.

ACKNOWLEDGMENT

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Magnetic-less converter based on Piezoelectric Transformers for step-down DC/DC and low power application

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***Abstract*- This paper presents a very simple step-down DC/DC low power converter based on Piezoelectric Transformers (PTs) without any magnetic component. PTs become very interesting in this kind of applications comparing with magnetic transformers due to the higher power density. It is important to highlight that the PT has been specifically designed to avoid the use of magnetic components. Dynamic response of the power stage with the PT is analyzed, achieving a 2.5 kHz bandwidth. The use of a PT allows a wide input voltage range (20 V - 75 V), 3 V, 1 W DC/DC converter.**

I. INTRODUCTION

During the last years the miniaturization of low power AC/DC and DC/DC converters are an important trend. Piezoelectric Transformers (PTs) provide several advantages comparing with magnetic ones in this kind of applications due to higher power densities, absence of electromagnetic noise, higher isolation voltages, high voltage conversion ratio and wide input voltage variation.

Unfortunately, most of the developed converters need the inclusion of extra magnetic components in order to make the PT work properly ([1]-[3]). These magnetic elements make the PT work under sinusoidal conditions.

Although the optimum behavior of PTs is obtained by applying a sinusoidal waveform, it is possible to drive a PT with square voltage. Although this solution is not the optimum from the PT point of view, it allows optimizing the whole converter, keeping PT efficiency good enough ([5]). It is important to highlight that the goal is to reduce the size of the converter for this particular application. Therefore, the elimination of the impedance matching networks is the objective of this paper.

In this paper, a step-down DC/DC and low power converter without magnetic elements is presented. The elimination of magnetic components is possible thanks to a suitable design of the PT.

II. PIEZOELECTRIC TRANSFORMER ISSUES FOR MAGNETIC-LESS CONVERTER

PT design is intended to achieve Zero Voltage Switching condition (ZVS) to optimize the whole converter even though PT performance is penalized.

The considered working mode of PT is thickness extensional mode. The PT resonance frequency is inversely proportional to the thickness dimension of the device. Therefore, the lower the PT thickness, the higher the PT resonance frequency. The input impedance magnitude and phase of a PT are plotted in Figure 1. The operating frequency range of the PT is located between resonance (f_{res}) and antiresonance (f_{ares}) frequency of the considered vibration mode, where the PT is able to transfer energy efficiently.

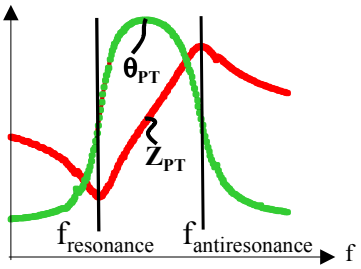

Figure 1. Magnitude (Z_{PT}) and phase (θ_{PT}) of the input impedance of the PT versus frequency. Operating frequency range.

In order to develop a competitive converter, the selected topology is the one shown in Figure 2, which is a topology widely used in PT applications.

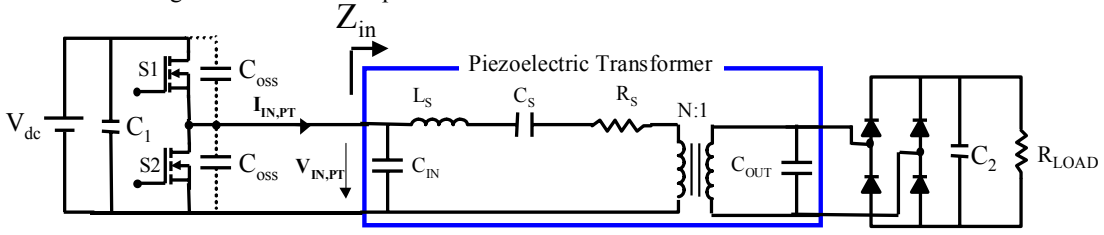

Figure 2. Power topology.

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The inverter stage is based on Half Bridge (HB) topology. The PT fixes the switching frequency of the HB within its operating frequency range.

PT works very well in sinusoidal conditions with high efficiency (98 %) and high power density (over 500 W/inch^3). Nevertheless, sinusoidal waveforms in the PT require the use of bulky resonant elements. A simpler converter can be obtained by applying square waveforms to the PT, although hard voltage transitions are produced.

Soft voltage transitions at the PT input are needed to have good performance of the PT ([5]). Although PT design for ZVS condition penalizes PT efficiency, it makes possible to eliminate the additional magnetic elements (impedance matching) required to achieve ZVS condition. In addition to this, ZVS condition becomes critical in order to reduce the switching losses and to increase the converter efficiency since HB is operating at high frequencies.

Since PT is driven with square voltage that contains harmonics of several orders, PT design should minimize the magnitude of other vibration modes. If the high order harmonics of the input voltage produce spurious modes, PT performance worsens because it vibrates in different directions.

Finally, the PT electrical parameter that accounts for the transferred power is the input conductance (G_{PT}) that is the real part of the input admittance. Given a PT power (P), the input voltage (V_{IN}) that can be applied to the PT is related to the input conductance (G_{PT}) according to the following expression:

$$P = G_{PT} \times V_{IN}^2 \qquad (1)$$

The converter control law can be drawn from the PT input conductance (Figure 3): an increment in the input voltage of the converter involves an increment in the switching frequency of the converter in order to keep constant the power supplied to the load.

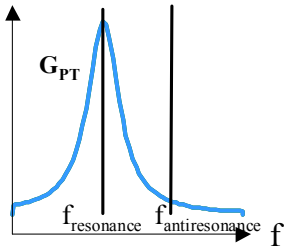


Figure 3. Input conductance of PT versus frequency.

One important aspect, from the point of view of the control loop of the converter is the variation of the input conductance with the load.

Figure 4 shows the input conductance of PT for the three main cases of load condition: short circuit condition, open circuit condition and the optimum load. For the optimum load (solid line), an increment of the switching frequency is required in order to keep constant the output conditions of the converter when there is an increment of the input voltage (from A to B point). But, if there is a reduction in the output load of the converter (open circuit condition, dashed line) the PT crosses a dangerous point (C point) because of the high increment of the PT input power. In addition to this, there is change of the PT control law. Hence, a phase control added to a frequency control is required to avoid these two situations.

Nevertheless, the PT needs to be designed to operate from this minimum frequency in order to implement simple frequency control. That means to reduce the PT operating frequency range, but to improve the converter in terms of size and complexity.

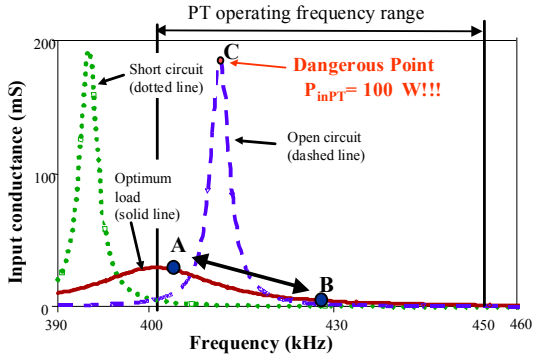


Figure 4. Input conductance of the PT for different load conditions.

It is important to notice that the input impedance phase decreases near the resonance and antiresonance frequency. That is, the PT is not able to supply the required inductive behavior to achieve ZVS. Therefore, a reduction of the theoretical operating frequency range, located between the resonance frequency and the antiresonance frequency, is obtained due to hard voltage transitions at the input of the PT.

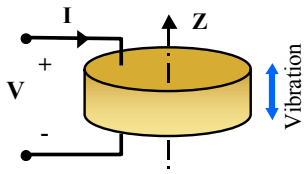
In addition to this, the efficiency of the PT decreases in the vicinity of the resonance frequency. That means, there is an increment of the losses in the PT that can produce an overheating of the PT. Due to this fact, the PT can not work at the required power level in these frequencies ([4]). Therefore, a reduction of the theoretical frequency range is obtained to keep the power level of the application.

To summarize, there is a trade-off in PT design related to PT efficiency, the inductive behavior of the PT and the input voltage range. In fact, wider input voltage variation can be obtained by reducing power level transferred by the PT and reducing PT efficiency, too.

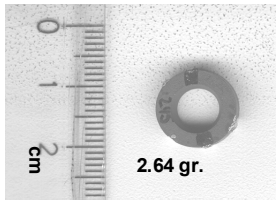
Therefore, the PT design specifications that must be considered are: the input conductance value (G_{PT}) necessary to transfer the required power level, the inductive behavior (θ_{PT}) to provide ZVS to the HB stage, high efficiency and the reduction of the spurious modes due to square driving.

The described features can be obtained selecting the suitable values of the area, the length, the number of layers, the thickness of the layers and the position of this layers of the PT as it is explained in [6].

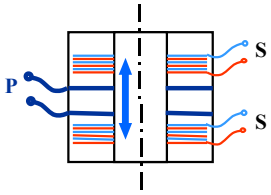
The optimization of the PT electrical features can be achieved by the use of the interleaving of the electrodes ([7]).



a. Working mode



b. External shape



c. Electrodes distribution

Figure 5. Sample features

III. PIEZOELECTRIC TRANSFORMER SAMPLE DESCRIPTION

These concepts have been validated with a sample that is not specifically designed for this application.

The physical characteristics of the sample are the following:

- The **working mode** is the first order of **thickness extensional mode**. The electrical field that is generated by the applied voltage (V) is in Z-axis direction. As it is shown in Figure 5.a), the vibration direction is coincident with the electric field direction.
- The prototype transformer has been manufactured using **PZ26 material** ([8]).

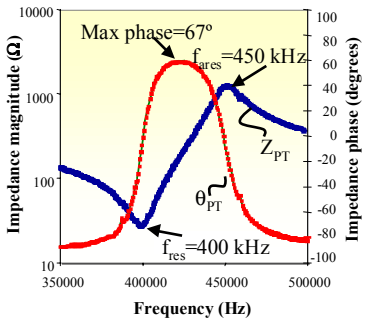


Figure 6. Input impedance magnitude and phase of the PT with its optimum load.

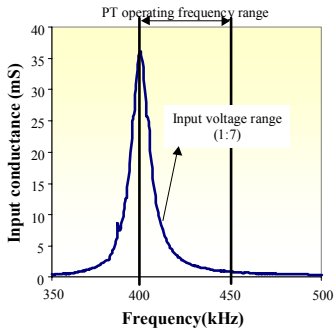


Figure 7. Input conductance with the optimum load

- It is a **ring-shaped block** which transversal area is 63 mm^2. Its thickness is 4 mm to establish an operating frequency of the inverter switches around 400 kHz. The selected frequency keeps a trade-off between switching losses of power topology and PT size. The external dimensions and shape are shown in Figure 5.b.
- **Interleaving of** the primary and secondary **electrodes** (Type I, see Figure 5.c) has been used in order to avoid spurious modes, increase input voltage variation, have high PT efficiency and provide good inductive behavior ([7]). There are bulk areas in order to adjust the length of the transformer to the frequency and also to reduce spurious modes.

The resistive load that presents the maximum efficiency in the PT is named optimum load (R_{opt}). The R_{opt} of this sample is 5 ohms. The small signal features of this sample with its optimum resistive load are shown in Figure 6 and Figure 7. As seen, the working frequency range is located between 400 kHz and 450 kHz that are the resonance and antiresonance frequency respectively. The k_{eff} value is 46 % and the input voltage variation taking into account (1) is 1:6.9.

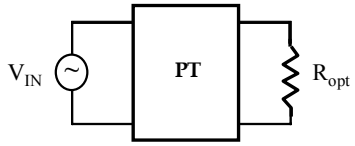


Figure 8. Power test: Sinusoidal driving conditions.

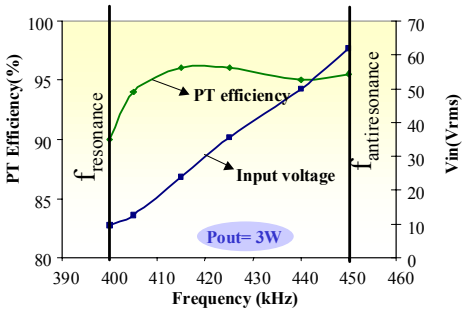


Figure 9. Measured efficiency and input voltage variation. Sinusoidal driving test.

Sinusoidal driving test of the sample (Figure 8) with the optimum load has been done in order to evaluate its efficiency and its operating input voltage range under large signal conditions. As seen in Figure 9, the efficiency plot is rather flat and the value is high enough in the operating frequency range except close to the resonance frequency due to the operating vibration order of the device (first order of the thickness extensional mode). As it is shown, this sample is able to transfer 3 W under sinusoidal conditions with an input voltage variation from 9.5 Vrms to 62 Vrms (1:6.5). This sample has a power capability of 6 W with an efficiency of 96 % operating at constant input voltage. However, this large variation of the input voltage

limits the power capability of the application. Therefore, there is a trade-off between power capability and input voltage range of the application.

In addition to this, square voltage conditions penalize the PT efficiency comparing to sinusoidal conditions (from 96 % to 90 %). That means to reduce the power capability of the sample in order to keep a wide input voltage range.

IV. Power Topology Design

The simplest topology where the PT can be included has been considered to choose the topology. Taking into account the Mason's model of the PT (Figure 10), resonant topologies are the most suitable ones. Class-E topology needs only one switch but the main drawback is the required big inductor. In addition to this, higher breakdown voltage switch is needed and lower converter efficiency is obtained. Therefore, a class-D topology (Figure 2) has been chosen in order to develop a competitive PT converter. The disadvantages of this topology comparing to class-E are the higher number of the switches and the floating control terminal.

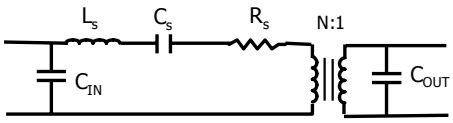


Figure 10. Mason's model of the PT

The topology needs an inverter stage at the input of the PT to transforms the input DC voltage to the AC voltage of the PT resonance frequency. A rectifier in the PT output is needed to supply the DC voltage to the load. It is important to notice that all the components of the converter have been chosen to obtain the lower converter size.

A. Inverter stage.

The MOSFETs of the inverter are placed in Half Bridge (HB) configuration, therefore the voltage in the output of HB is a square voltage that varies between maximum input voltage value (V_{dc}) and 0 V.

The switching frequency of the MOSFETs is fixed by the operating frequency of the PT, that is between 400 kHz and 450 kHz. Since switching losses are very important due to this high switching frequency, ZVS condition is required.

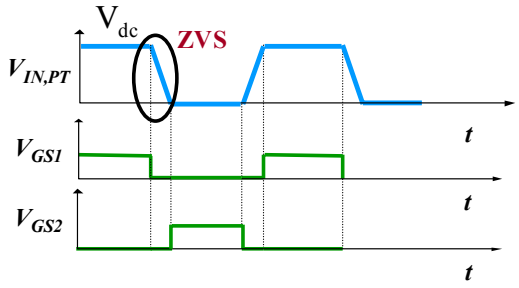


Figure 11. Gate-source MOSFETs voltage and PT input voltage waveforms.

Both switches are turned on and turned off alternatively with a short dead time (Figure 11). This time is required to discharge the MOSFETs capacitance (C_{oss}) and the large PT input capacitance (C_{IN}). Therefore, soft-switching transitions of the input PT voltage ($V_{IN,PT}$) are obtained. This means that MOSFETs with low parasitic capacitance must be selected.

In addition to this, MOSFETs must be able to support maximum input voltage value (V_{dc}).

B. Rectifier Stage.

The voltage at the output of the PT is an AC voltage of the PT operating frequency. There are two rectifiers without magnetic elements that can be used to obtain the required DC voltage: Half-wave and a Full-wave rectifier.

As mentioned before, the PT has the maximum efficiency when it works with its optimum load. The equivalent resistive load seen by the PT is different with each rectifier. The equivalent resistive load of half-wave rectifier is $(2/\pi^2)*R_{LOAD}$ that is lower value that Full-wave equivalent resistive load ($(8/\pi^2)*R_{LOAD}$).

On the other side, half-wave rectifier implies less number of rectifier devices increasing converter efficiency. Nevertheless, lower equivalent PT load requires higher number of layers in secondary side and bigger PT area ([6]). Since there is an increment of price and size of PT, Full-wave rectifier has been chosen.

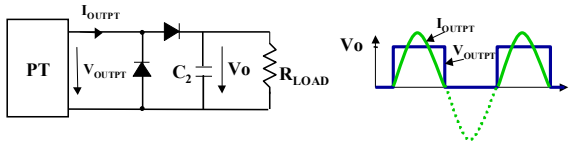


Figure 12. Half-wave rectifier.

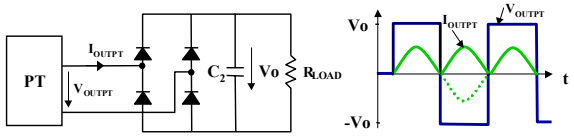


Figure 13. Full-wave rectifier.

Rectifier devices have to work at high frequencies. In addition to this, low forward voltage (V_F) is desired in order to increase converter efficiency.

Finally, a capacitor (C_2) is added in order to filter output voltage harmonics. This device must be able to support output voltage value (V_0) and to achieve the required output voltage ripple.

V. Dynamics Analysis: Control Loop Design

Once the power topology is designed, a control loop is necessary in order to keep constant the output voltage that must be applied to the load. As it has been mentioned in paragraph II, a frequency control of the converter involves the simplest control loop design. In order to have the required output voltage, the control loop must fix the proper switching frequency of the HB.

The block diagram of the converter with the control loop is shown in Figure 14. Output voltage of the converter is measured by an optocoupler to keep the electrical isolation

between input and output. Comparing the output voltage with a reference (V_{ref}), the Voltage Controlled Oscillator (VCO) and the regulator determine the switching frequency of the inverter. A driver is necessary to generate the required gate-source signals of the MOSFETs (Figure 11).

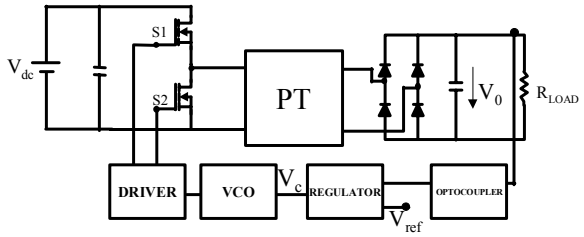
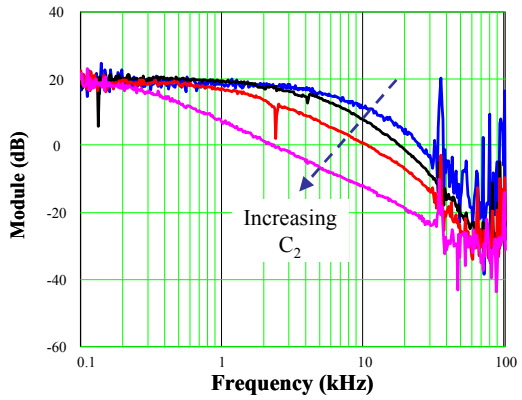


Figure 14. Block diagram of the converter.

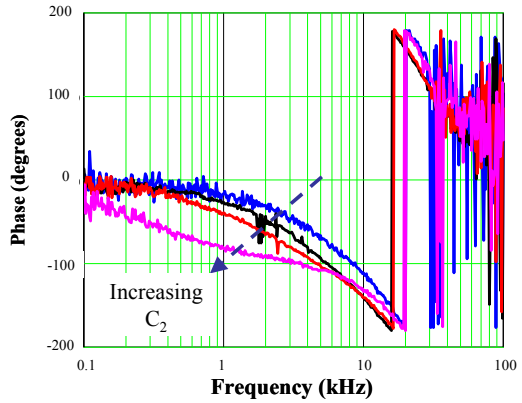
In this section, the features of the regulator for this application are detailed.

A. Analysis of power topology

The selection of the output capacitor (C_2) has an important influence on the power stage dynamics. Figure 15 shows the magnitude (a) and phase (b) of open loop response of the power topology. The considered values of C_2 are: 4.7, 10, 20 and 120 µF.



a. Magnitude



b. Phase

Figure 15. Measured open loop response of the power stage. Influence of C_2.

As seen, C_2 changes the position of the system poles. The higher the value of C_2, the lower the pole frequency.

Furthermore, the influence of this capacitor must be taken into account in the PT design to optimize the features of the power topology.

A value of 120 µF for C_2 has been selected in order to obtain an adequate transient response of the converter. This feature will be shown in the experimental results of the converter.

B. Regulator design.

In order to design an adequate regulator, the open loop response of the power topology has been measured (Figure 16). The measured transfer function relates the output voltage of the converter (V_0) and the VCO voltage (V_c) that determines the operating frequency of the converter.

As seen in Figure 16, the phase of the measured function versus frequency starts decreasing quickly around 6 kHz while the module decreases more slowly. That means the system behaves as it has a right half plane zero at this frequency. Due to this fact, the application bandwidth is limited to half of the zero frequency [9].

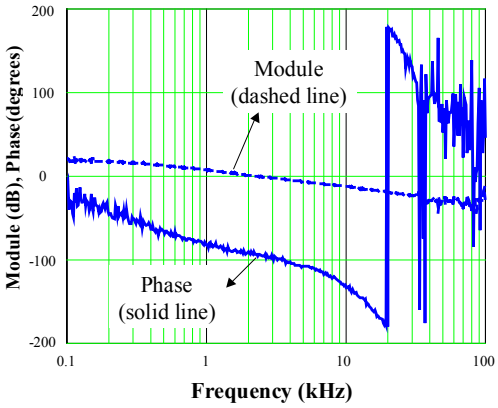


Figure 16. Measured open loop response of power topology

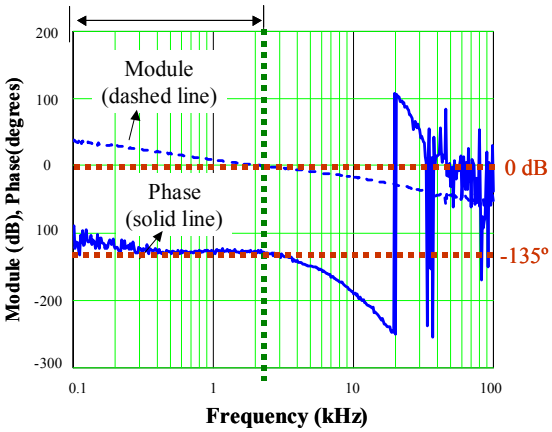


Figure 17. Open loop response of the power topology with the regulator.

Type II regulator has been chosen in order to eliminate the position error and to obtain the maximum application bandwidth. The open loop response of the converter with the designed regulator is shown in Figure 17. From this

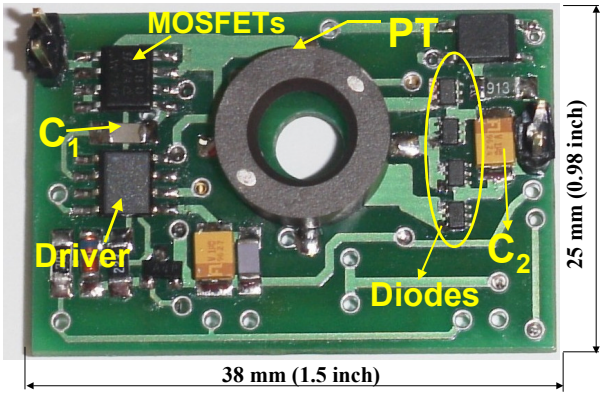
plot, it can be seen that the system is stable since a margin phase of 45º is obtained while its bandwidth is 2.5 kHz.

VI. Experimental Results

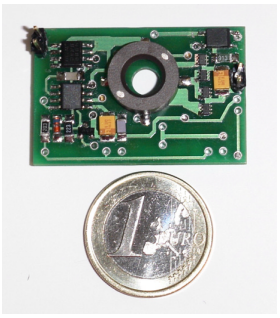
A prototype with the described topology and sample has been developed. Using the available sample, the following specifications have been selected to validate previous concepts:

- Input voltage: 20 V - 75 V DC voltage.
- Output voltage: 3V DC voltage.
- Output load: 50 mW - 1 W.

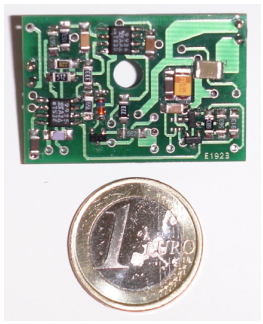
In Figure 18 is shown the converter prototype. The size of the converter is (LxWxH) 38x25x7 mm^3 (1.5x0.98x0.276 $inch^3$). It is important to highlight that the aim of this converter is to develop a converter without magnetic components. Therefore, the components and PCB technology (two layer PCB) have not been optimized in terms of size.



a. Components of power topology.



b. top side



c. bottom side

Figure 18. Prototype of the converter.

Taking into account the mentioned specifications, the components used in the prototype are:

- Both input MOSFETs are in the same SO-8 package (Si4980DY). Maximum drain-source value is 80 V; On-resistance R_{DS}= 75 mΩ and maximum drain current value is 3.7 A.
- Four rectifier devices have been used. The size of each device is SOT-666. The forward voltage (V_F) is 0.3 V and they are able to work properly at high frequencies.
- Input capacitor (C_1) has a 1210 case package and its capacitance value is 220 nF for 100 V of maximum voltage. Output capacitor (C_2) consists on two capacitors: a tantalum capacitor of 100 µF and a ceramic capacitor of 20 µF. The size of the tantalum capacitor is a case C package (W=3.2mm, L=6mm, H=2.6mm) and the size of a ceramic capacitor is 1210 case package. Both capacitors are for 6.3 V of maximum voltage value.

The measured converter efficiency is rather flat and over 60 % as it is shown in Figure 19. The low efficiency is due to the rectifier stage because of the low output voltage and low power application. Nevertheless, it is important to notice that efficiency is not the objective of this application.

Another important feature of the converter is the comparison of the power stage efficiency under maximum load (1 W) and minimum load (50 mW) conditions. As seen in Figure 20, the converter is able to work under 50 mW of minimum output power, which is very close to no load condition.

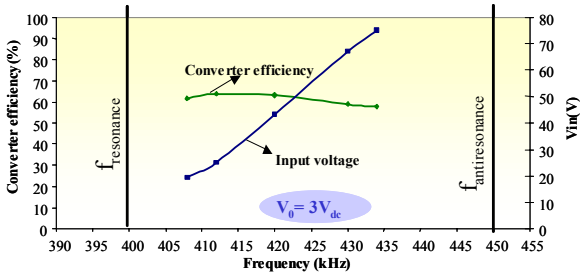


Figure 19. Measured power stage efficiency at maximum load (1 W).

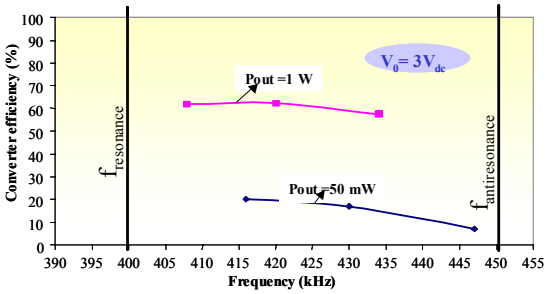


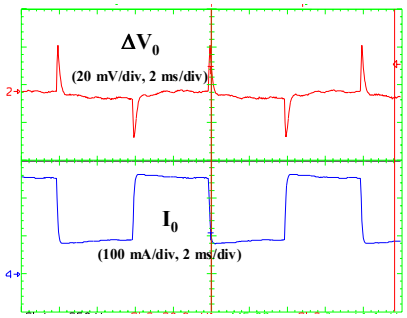
Figure 20. Measured power stage efficiency at maximum (1 W) and minimum load (50 mW).

In addition to steady state measurements of the converter, the transient response has been measured. The load of the converter has been changed from full to medium load.

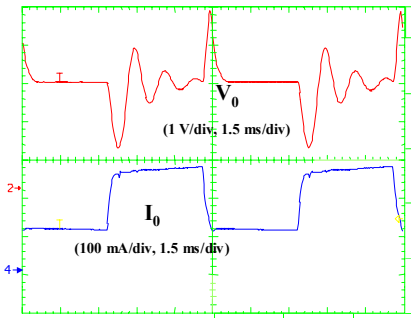
The measured transient response with different capacitance values of C_2 (120 µF (Figure 21.a) and 10 µF (Figure 21.b)) and the same system bandwidth (2.5 kHz) has been analyzed. As seen in Figure 22, lower C_2 value increases dramatically the output voltage ripple (from 44 mV to 4 V). With lower C_2 and the same system bandwith, the PT must provide higher current to the output capacitor during the transient to keep constant the output voltage. The transient response of Figure 21.b shows that the PT can not

provide the required current with lower C_2. The system enters into non-linearity and the converter response is asymmetric. The PT response is damped under a step-down load variation. The frequency behavior of the PT (Figure 3) explains this asymmetric transient response

As seen in Figure 21, the measured transient response of the converter agrees with the designed system bandwidth. Therefore, the proposed methodology for the control loop design has been validated.



a. C_2=120 µF.



b. C_2=10 µF.

Figure 21. Measured transient response of the converter.

VII. CONCLUSIONS

A DC/DC converter prototype for 20 V - 75 V DC input voltage range, 3 V DC output voltage and 1 W output power has been tested. The main feature of this converter is the use of a Piezoelectric Transformer (PT) without any additional magnetic element.

Half-bridge inverter topology with a full-bridge rectifier stage has been chosen because it drives properly the PT. Furthermore, proper PT design, that takes into account the topology constraints, avoids the use of magnetic elements as well as provides ZVS operation. The PT can deliver 6W (96% PT efficiency) under sinusoidal conditions, and if it is driven with a soft-squared waveform the maximum power is reduced down to 3W (90% PT efficiency). However, sinusoidal driving of the PT requires a complex topology with additional magnetic elements, while soft-squared driving improves the overall converter in terms of size and weight since no magnetic elements are necessary. The cost paid by operating with a wide input voltage range (1:3.75) is also a reduction of the power capability of the PT (from 3W to 1W). Although power stage efficiency is 60%, the obtained results are good enough taking into account the low output voltage (3 V) and low output power (1 W). In addition to this, the absence of electromagnetic noise are obtained.

The analysis of power stage dynamics shows a right half plane zero behavior that limits the application bandwidth around 2.5 kHz.. However, a proper selection of the output capacitor plus the adequate design of the regulator allow achieving a good dynamic regulation. The measured output voltage variation is ± 22 mV under medium – full load steps.

It is important to highlight that the PT has not been designed for this application. Therefore, further improvement can be obtained with a PT specifically designed for these specifications.

Therefore, the concept of using a PT without magnetic components has been validated. PT technology has allowed to obtain a low profile converter (7 mm) for a low power (1 W) and low voltage application (3 V) with a wide input voltage range (1 : 3.75).

ACKNOWLEDGEMENTS

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